DIGITAL RECEIVER SUB-SYSTEM STUDY

FINAL REPORT

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1.0 INTRODUCTION

The study of the digital receiver sub-system was performed by TELEMUS Electronic Systems Inc. under a contract for the Defence Research Establishment Ottawa, Communications EW Group. Essentially the purpose of the contract was to perform a detailed hardware oriented study of the various sub-systems of a hybrid analog and digital broadband communications ESM surveillance receiver. A brief overall system study in which the interaction of the various sub-systems was examined followed. Activity completed on the study with the compilation of this report, detailing the results of the analysis performed over the duration of the contract.

The report has been divided into several sections essentially representing the sub-systems forming the receiver. Section 2 reviews the technology while Section 3 covers overall system considerations. Section 4 provides conclusions from the study and recommendations for future work. A list of references are provided in Section 5 and a number of appendices are provided to assist the reader in identifying and defining specific technical considerations and terms.

2.0 TECHNOLOGY OVERVIEW

2.0.1 Scope

This section of the report is divided into three sub-sections detailing :

- Front End Technology
- Analog to Digital Conversion, and
- Digitization.

Each section has been written such that it could be extracted from the report and used as a stand alone document.

The communications ESM receiver discussed in this report was intended to intercept transmissions in the VHF band in the frequency range 30 to 88 MHz. An essential part of the receiver system, not included in this study, is the antenna sub-system. The performance of the antenna sub-system has been assumed to be sufficient to permit optimising of subsequent equipment to meet the required operational performance.

2.0.2 General Considerations

Current communications ESM receivers have to operate in a dense and increasingly complex emitter environment. This has made escalating demands on the overall performance requirements expected from these receivers. In a conventional sense the need to be able to extract a weak signal in the presence of a stronger one has lead to demands for a receiver to have a spurious free dynamic range of the order of 100 dB in a dense environment. Multiple short duration emitters combined with the use of frequency agility (hoppers) drives the receiver requirements towards wide bandwidths in order to maintain a reasonable probability of intercept (POI). The growing lethality of the environment intensifies the concern over mobility and hence the need for antenna systems which are small and portable, but at the same time being able to provide acceptable DF accuracy. Alternatively, high DF accuracy forces the deployment of assets to elevated platforms, such as aircraft or helicopters.

It is with these issues in mind that various attempts have been made to apply technology to improving a communication ESM receiver's performance. Currently a number of receiver types have been considered :

- Superheterodyne - detector/discriminator
- Microscan
- Acousto-Optic.

Each of these receiver types deals with the environment with greater or lesser degrees of success. Limited frequency coverage, or limited dynamic range has diminished the attraction of these receiver types, although each has benefited from improvements in technology. However, the rapid and continuous advance of technology has made a new type of receiver increasing more attractive and viable. This type of receiver is known as a digital receiver.

2.0.3 The Digital Receiver

The digital receiver essentially makes use of pre-detection digitization and hence recording. That is the signal is digitized and stored at radio frequencies. A variation on this type of receiver digitizes at an intermediate frequency. The other types of receiver use digitization but this is usually done post detection. The advantage of pre-detection digitization rests in the fact that none of the information is lost in the process, which is not the case with post-detection recording. A second advantage to the digital receiver approach is the flexibility it offers in signal processing. Once stored in memory the whole signal with all its facets can be processed using a variety of powerful techniques.

The key technology in this type of receiver is the high speed digitizer which includes the analogue to digital converter. TELEMUS has considerable experience in the design and application of this type of technology, examples of these are mentioned in the reference. Much of this background has been as a direct result of support through contracts won by TELEMUS from DREO, and thus this report has benefited from the amassing of this knowledge within the company.

A digital receiver may implement digitization directly after a simple pre-amplifier/filter front-end or at some intermediate frequency the value of which is determined by the bandwidth requirement and detailed receiver design trade-offs which are discussed in Section 2.3. Suffice to say that a super-heterodyne receiver usually takes the form of either single or dual down conversion, or up/down conversion.

During a detailed receiver design, the designer may also consider the use of narrowband, broadband or channelized receiver super-heterodyne architectures or a combination of these. An alternative frequency conversion scheme is frequency division, this technique affects modulation information and would only be considered for systems where carrier information was the only parameter of interest.

2.1 Front End Design

An analysis is presented on the analog hardware associated with the front end of a communications receiver, reviewing alternate design approaches. Several design approaches are identified and these are followed by an analysis of the component technology relevant to each of these designs.

Frequency translation techniques applicable to the frequencies under consideration are effectively completely displaced by the superhetrodyne receiver. As the input signal frequency increases, other techniques tend to show favour but certainly in the VHF band, the superhetrodyne technique dominates. Therefore, only the superhetrodyne design approach was considered during this study.

2.1.1 Superhetrodyne Receivers

Consider the function and structure of a superhetrodyne receiver, as illustrated in Figure 2.1.1 which shows a basic superhetrodyne receiver functioning in the following manner. The object here is to transfer the incoming signal down in frequency to a baseband to ease subsequent processing. A mixer circuit is used to accomplish this. The LO generates a CW signal f_l. If the input signal frequency f_s is fed to the mixer, then f_s will be shifted to f_i, the difference frequency of f_l and f_s. An IF filter following the mixer is a bandpass filter which is used to pass the desired IF signal and stop all other frequencies generated in the mixer. The IF amplifier following the filter provides most of the gain of the receiver. Following the IF amplifier is a video detector converting the IF signal to a video signal. A video amplifier may follow the detector to amplify the video signal for further processing.

Variations on this configuration improve the basic operation of the receiver. A preselector placed before the mixer can be used to filter out unwanted signals before they get to the mixer and cause spurious frequencies. Additional stages of amplification can be used to improve the system dynamic range and sensitivity. Each additional stage would have associated with it, a bandpass filter to improve spurious signal rejection. Automatic gain control may be used in the system to prevent saturation of any of the amplifiers, thereby maintaining the integrity of the processed signal but reducing the system dynamic range as a consequence. Figure 2.1.2 shows such an arrangement. In practice, mixers operating at these frequencies often have an amplifier built into the circuit within the integrated package and therefore the filter can be placed directly after the mixer.

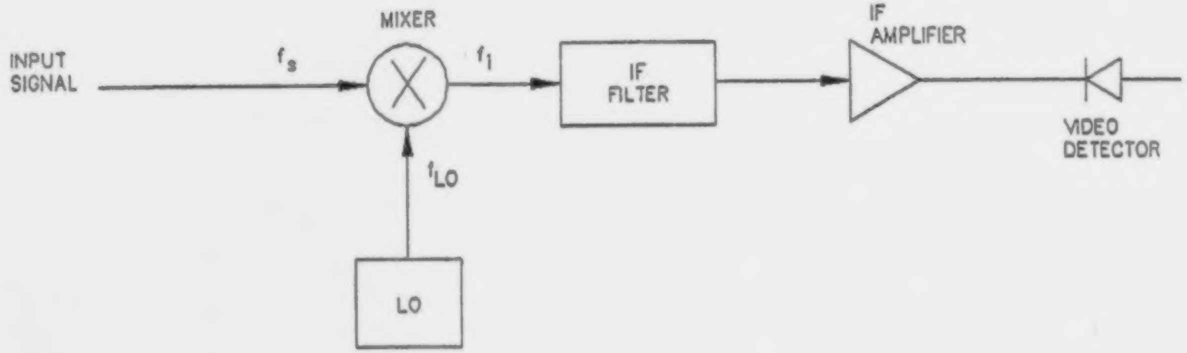


FIGURE 2.1.1 BASIC SUPERHETRODYNE RECEIVER

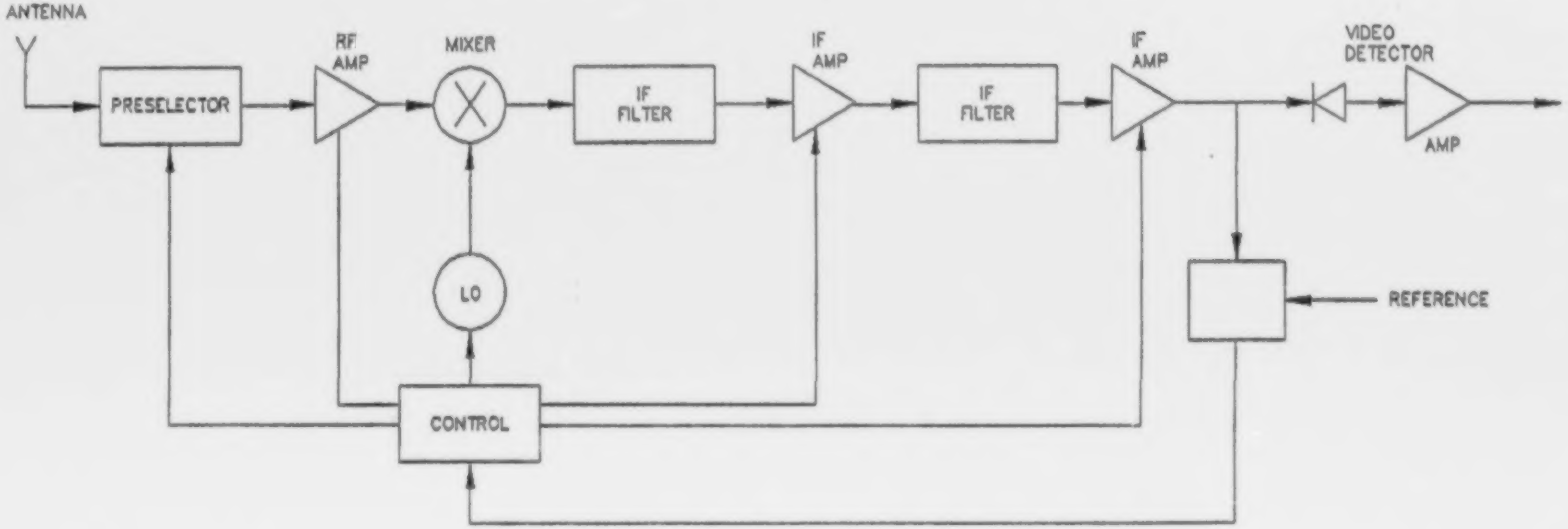


FIGURE 2.1.2 TYPICAL SUPERHETRODYNE RECEIVER

Consider the options of front end design. As the application calls for a broadband receiver, certain design features have to be included. The Local Oscillator has to be tuned over a range of frequencies to enable a constant IF frequency to be utilised. The tuning rate of the LO becomes a critical factor leading to a determination of the probability of interception and detection.

The essential performance characteristics of the more critical components have a significant impact on the overall performance of the receiving system. To that end, the more critical components have been studied and an evaluation carried out on their salient characteristics.

2.1.1.1 Filters

One or more stages of mixing would be designed into the communications receiver depending on the level of resolution required on the intercepted signal. Each mixing stage would be fed from a bandpass filter and followed by a bandpass filter to minimise spurious signal generation. The LO frequency would be selected to produce a constant IF baseband for subsequent processing.

The pre-selector or bandpass filter may be of a fixed bandwidth and tuneable over the system frequency coverage. A pre-selector must reduce the receivers' response to the image frequency (twice the intermediate frequency away from the desired signal) and reduce the radiation of the receivers' LO out of the receiving antenna. Further, the pre-selector aids in reducing the receivers' response to the IF and its sub-harmonics as well as providing rejection to spurious signals caused by the mixing process.

For broadband receivers, the pre-selector has to be tunable but for narrowband receivers the pre-selector may cover the entire band of interest. Modern communication receivers tend to follow the tuneable pre-selector type due to frequency diversity and agility techniques presently in use. In a typical down converter, both the LO and image frequencies can lie in the desired band and the IF is out of band.

Often the pre-selector tuning is ganged with the LO tuning to ensure adequate tracking between the input signal filtering and the mixer spurious signal generation. This tuned pre-selection design may be implemented by using one or more pre-selectors depending on the tuning range required. Tuning traditionally has used a mechanical approach by altering capacitance or inductance but the trend is now to tune electronically using varactor diodes or direct digital switching under digitally linearized control.

The pre-selector may be derived from one of several forms of filter technology. Essentially, the pre-selector must have a flat passband and extremely high attenuation outside the passband. Given the operational frequency range for this receiver study, LC, crystal, ceramic, and surface acoustic wave (SAW) filters could be used for these applications. Table 2.1.1 illustrates filter construction techniques and related parameter data.

Many filters are commonly available up to 88 MHz and can be selected to conform to the Chebychev, Bessel or Butterworth characteristics. The number of poles has to be determined which identifies the level of attenuation expected outside the pass band. Appendix A shows some general data on bandpass filters from K & L.

Table 2.1.2 illustrates the common filter characteristics for the Chebychev, Bessel and Butterworth designs. As can be seen, the selection of the filter type depends on the specific application, that is, fastest out of band attenuation, linear phase in the passband or maximally flat passband.

For this application, filters are required in several system locations. The RF bandpass filter which would be located after the antenna has to pass the 30 MHz to 88 MHz signal. Various

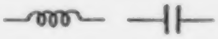
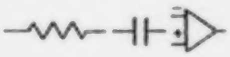
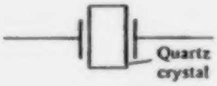
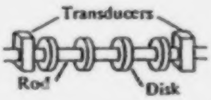
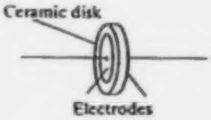
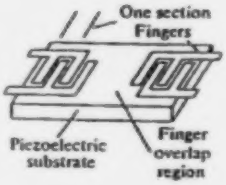
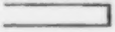
Construction Type	Description of Elements or Filter	Center Frequency Range	Unloaded *Q* (Typical)	Filter Application[a]
LC (passive)		dc–300 MHz	100	Audio, video, IF, and RF
Active		dc–500 kHz	200[b]	Audio
Crystal		1 kHz–100 MHz	100,000	IF
Mechanical		50–500 kHz	1,000	IF
Ceramic		10 kHz–10.7 MHz	1,000	IF
Surface acoustic waves (SAW)	 One section Fingers Piezoelectric substrate Finger overlap region	10–800 MHz	[c]	IF and RF
Transmission line		UHF and microwave	1,000	RF
Cavity		Microwave	10,000	RF

TABLE 2.1.1 FILTER CONSTRUCTION TECHNIQUES

Type	Optimization Criterion	Transfer Characteristic for the Low-Pass Filter*
Butterworth	Maximally flat: as many derivatives of $\lvert H(f)\rvert$ as possible go to zero as $f \to 0$	$\lvert H(f)\rvert = \frac{1}{\sqrt{1 + (f/f_b)^{2n}}}$
Chebyshev	For a given peak-to-peak ripple in the passband of the $\lvert H(f)\rvert$ characteristic, the $\lvert H(f)\rvert$ attenuates the fastest for any filter of nth order	$\lvert H(f)\rvert = \frac{1}{\sqrt{1 + \epsilon^2 C_n^2(f/f_b)}}$ ϵ = a design constant; $C_n(f)$ is the nth order Chebyshev polynomial defined by the recursion relation $C_n(x) = 2xC_{n-1}(x) - C_{n-2}(x)$ where $C_0(x) = 1$ and $C_1(x) = x$
Bessel	Attempts to maintain linear phase in the passband	$H(f) = \frac{K_n}{B_n(f/f_b)}$ K_n is a constant chosen to make $H(0) = 1$ and the Bessel recursion relation is $B_n(x) = (2n - 1)\, B_{n-1}(x) - x^2 B_{n-2}(x)$ where $B_0(x) = 1$ and $B_1(x) = 1 + jx$

*f_b is the cutoff frequency of the filter.

TABLE 2.1.2 GENERAL FILTER CHARACTERISTICS

approaches can be taken to achieve this. A single bandpass filter can be used which has a 58 MHz passband. Alternatively, a series of narrower band filters can be used to cover the 58 MHz band, each filter having a 4 MHz bandwidth. In this case, each filter could be switched into circuit thereby allowing flexibility in active frequency coverage. This may permit an improvement in system sensitivity and selectivity but at a reduction in the probability of intercept.

Should a variable tuned bandpass filter be selected then the filter would be controlled in accordance with the variations of the LO frequency. The varactor tuned or voltage tuned filter could be an LC filter where the capacitance is the variable supported by a varactor tuning diode. These filters are usually two or four pole designs, or cascades of two or four pole filters. Tracking of the individual filters becomes a problem as more poles are used. A tuning linearizer element is often incorporated into the system for remote tuning purposes.

The varactor tuning diode is one where the diode capacitance is controlled as a function of reverse bias, where the operating range of such a device is from cutoff to below reverse breakdown. The Q of the diode should be optimized and high Q is more easily obtained with diodes which have lower breakdown potentials. Typically the filter design incorporates diodes in groups of two in a back to back arrangement to lower distortion and improve dynamic range.

The IF bandpass filter would be fixed frequency and probably at a commonly used frequency, possibly 21.4 MHz (for a single stage down conversion). Standard components are available from several manufacturers. Subsequent stages of down conversion, should they be necessary, may utilize commonly accepted IF frequencies and therefore, common filter products would be available at reasonable cost. For ECCM purposes it may be undesirable to select IF frequencies that comply with commercial standards in order to increase the degree of difficulty for communications jamming.

2.1.1.2 Mixers

The frequency translation device, the mixer, is a device that requires two input signals and outputs a signal that consists of two principle components known as the sum and difference terms. Inputs to the mixer comprise the RF input signal and a Local Oscillator. In general, the LO power is higher than the RF input signal and is commonly arranged to be at a level 20 dB greater than the highest expected RF input signal power for down converters and at 10 dB greater than the highest expected RF signal for up converters.

Every mixer suffers from a conversion loss which is usually defined as the ratio of IF output power to signal input power. Conversion loss can be considered a measure of efficiency of mixer conversion between RF and IF energy. The noise figure of a mixer is equal to or slightly greater than its conversion loss. As a mixer has three ports, isolation between these ports is an important consideration. Isolation measures the power leaking from one port to another and figures for isolation between the RF/IF and LO/IF ports are generally provided by the manufacturer. In practice, the isolation between the RF and LO ports is important because poor isolation may lead to the LO radiating through the RF port.

A mixer is usually considered a linear component in a receiver but is not a true linear device in practice. Spurious outputs are generated by the mixer as well as the sum and difference terms of the true input signals. These spurious signals are the intermodulation products and harmonics of the input signals, so the mixer is followed by an IF bandpass filter which typically selects the difference signal and attempts to filter out all the other signals. Mixers take on several different forms that may employ diodes or transistors of bipolar or field effect design. They may be single ended, single balanced or double balanced mixers. The preferred design for optimum performance would be the double balanced mixer. Advantages of using a double balanced mixer are that of improving the port isolation, reducing the amplitude of spurious products and as a side product, of increasing the power handling capability of the mixer. When designing a receiver system, it is often found that driving the mixer with a square wave rather than some other waveform results in improved performance as the mixer sees a fast rising edge rather than a slow rising edge. This results in a design that experiences larger second and third harmonic signals from the mixer but improved performance overall.

Impedance matching at the mixer ports should be considered as part of the system design. Ideally, the mixer would be fed from a broadband amplifier and the IF signal would be fed to a bandpass filter then to an IF amplifier. Attenuators may be used in the mixer circuit to improve impedance matching and depending on the specific application, some matching may have to be included to permit impedance matching of signals outside the passband filter frequency coverage. The IF filter should be isolated from the mixer. Most mixers at these frequencies come complete with an internal amplifier, thereby providing the required isolation.

Termination insensitive mixers are available and are capable of handling strong received signals with good spurious performance. Image rejection mixers are available for applications where it may not be possible to filter out the image response and is thus treated as a valid in band signal. Image rejection of the order of 20 to 30 dB is possible with such devices.

In the article "Achieving Maximum Dynamic Range in a Modern Receiver" by Donald Steinbrecher, published in the September 1985 edition of the Microwave Journal, the paramixer was identified. This device is designed for maximum linearity and offers optimum performance in terms of minimal conversion loss and maximum dynamic range. Conversion loss was measured at about 6 dB and a third order intercept approaching +40 dBm was determined.

2.1.1.3 Amplifiers

To achieve the dynamic range required in a modern communications receiver, amplification has to be included in the system design. For this application there are two positions where amplifiers are to be found. At the input to the system, the effective bandwidth is that of the desired system coverage. A minimum coverage of 30 MHz to 88 MHz has been indicated for this study. The next type of amplifier required in the system is found after the mixer and operates at the IF frequency. Here the requirement is for an amplifier which operates over a narrow bandwidth, equal to the IF bandwidth.

From manufacturers data, bandwidths for amplifiers that conform to these requirements cover a frequency range much greater than the 30 to 88 MHz. The lower frequency of operation can be as low as 1 MHz but devices capable of operating at a minimum frequency of 10 MHz are much more readily available. For the upper operating frequency, values of 200, 400, 500, 1000 MHz and higher are available. Probably the most common operating frequency range identified from manufacturers data is 10 MHz to 500 MHz. Bandwidth is generally defined as the bandwidth lying between the two points having 0.707 of the voltage at the centre frequency. That is, the frequency band between the half power points. Conclusions are therefore that obtaining an amplifier that operates over the required bandwidth criteria does not present a problem. As the gain bandwidth product is a constant, therefore an amplifier operating over a wider frequency range than is needed will exhibit a lower gain parameter. The designer should attempt to limit the operating frequency range of the amplifier to closely match that of the actual requirement. This practice may lead to a reduction in the total output noise of the receiver system. Also, the roll off of the amplifier, if chosen carefully can play a part in the filtering characteristics of the receiver.

Any device operating above 0 degrees Kelvin will generate thermal noise and amplifiers are no exception. Devices are available that range from ultra low noise narrowband products exhibiting noise figures of the order of 1.5 dB to high gain cascaded amplifiers having noise figures between 7 and 10 dB. Other devices are available that have a very low noise figure but these are usually exotic cryogenic types and are not usually found in the types of receiver under discussion. Voltage controlled AGC amplifiers are available from several sources and the manufacturers quote noise figures at zero AGC. Such a device from Avantek, the AGC-553 has a 9 dB maximum noise figure at zero AGC but at the maximum AGC voltage of 5 volts, the noise figure increases to the order of 25 dB. This device utilizes a voltage controlled attenuator within an integrated circuit TO-8 package that leads to this level of noise figure.

The RF amplifier stage should be designed to exhibit a minimal noise figure as the first stage of a system has generally the greatest impact on the system noise figure. A system noise figure is defined as the input signal to noise ratio over the output signal to noise ratio and is expressed in decibels. Therefore the output signal to noise ratio encompasses all the noise contributions of the individual components that collectively make up the system. The system noise can be determined by using the equation below:

$$F_s = F_1 + \frac{F_2}{G_1} + \frac{F_3}{G_1G_2} + \frac{F_n}{G_1 \ldots G_{n-1}} \qquad \text{eq. (1)}$$

where F_s = system noise figure
F_n = noise figure for stage n
G_n = gain of stage n.

When the following stages have high gain, so the contributing factor to F_s is reduced and in many cases F_1 becomes the dominant factor. Noise figure and efficiency are closely tied together and therefore an efficient amplifier will exhibit a lower noise figure.

Amplifiers are required to operate in their linear mode so that unintentional distortions and intermodulation products are not created within the receiver system. In practice, although an amplifier can be designed to operate in the linear region each amplifier can only perform over a certain range in input signal level. As these limits of operation are approached, so the amplifier enters a non-linear range of operation which produces spurious signals.

A measure of the non-linear performance of an amplifier is provided by a determination of the second and third order intercept points. Figure 2.1.3 illustrates the relationship between the fundamental, second and third order slopes. Once these relationships have been established, the magnitude of any intermodulation product can be accurately predicted. From manufacturers data, third order intercept figures up to +40 dBm are available but this level of third order intercept is usually associated with relatively low gain and high noise figure. Given that the manufacturers data provides +40 dBm as a typical figure, then a third order intercept point of +45 dBm could be construed as being state of the art for medium power devices.

For this study, the receiver instantaneous dynamic range has been defined as the largest difference (in dB) between the power levels of two input signals for which the receiver is still able to detect the presence of the lower power signal. It represents the ability of the receiver to process two signals of significantly different power levels simultaneously. In practice, the two signals would be at different frequencies and instantaneous dynamic range should be defined for a given frequency accuracy, frequency

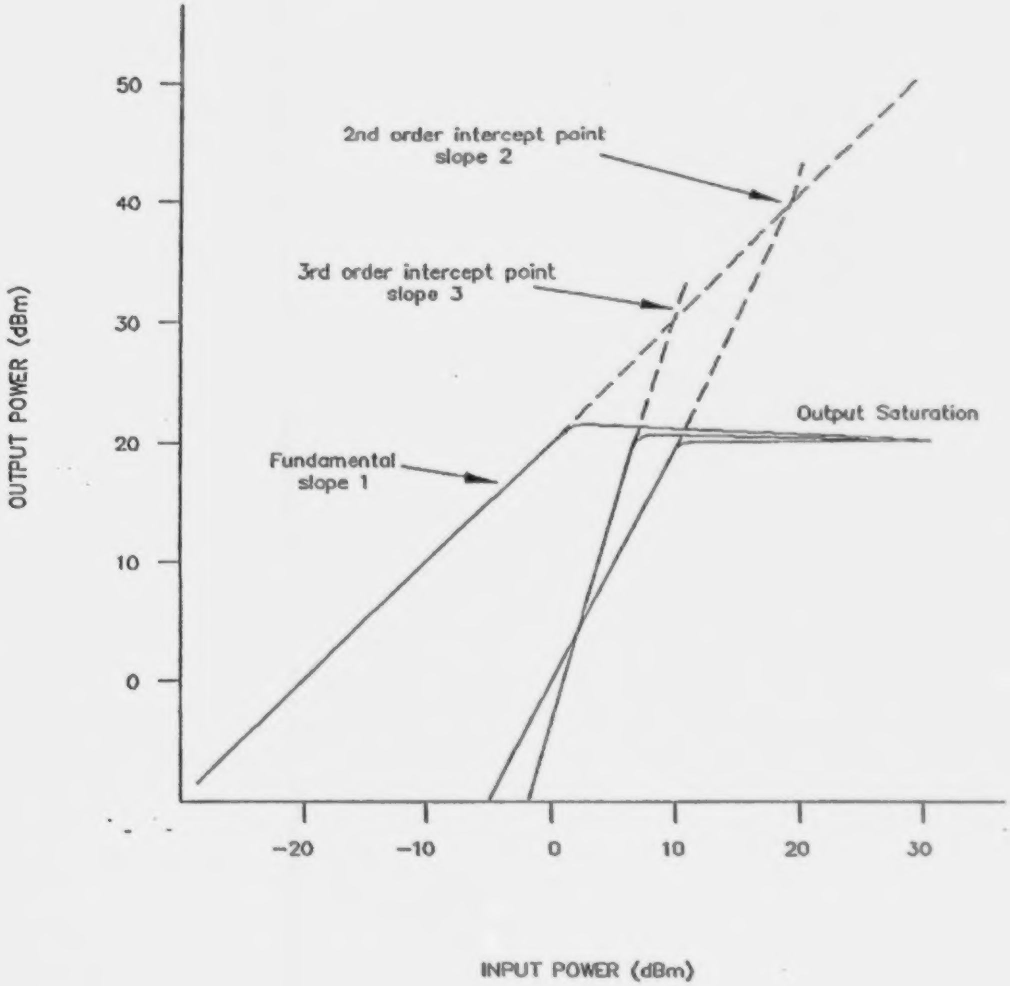


FIGURE 2.1.3 AMPLIFIER OUTPUT CHARACTERISTICS

separation between the two signals and a given signal to noise ratio.

Spurious free dynamic range has been defined as the dynamic range over which internally generated third order products, referred to the input, remain below the minimum discernable signal level of the receiver. The minimum discernable signal (MDS) has been defined as the input signal which causes a 3 dB (S+N)/N ratio at the detector input. A spurious free dynamic range can be related to the third order intercept point by:

$$\text{SFDR} = 2/3 \times (\text{IIP}^3 - \text{MDS}). \qquad \text{eq. (2)}$$

Any third order product which has a level above the MDS when referred to the input, will be processed as a valid signal. Both the instantaneous dynamic range and the spurious free dynamic range current capabilities will be discussed further in subsequent sections of this report.

Phase linearity represents the degree of deviation of the amplifier response from that of a true linear phase response and is usually measured in degrees. Manufacturing data indicates that amplifiers exhibit little deviation from linear phase except for when the input signal is of sufficient strength to drive the amplifier close to the saturation level. Deviations of less than one degree can be expected until the input power approaches the 1 dB gain compression point whereupon the deviation increases significantly as the input power continues to increase. To avoid significant phase deviation, the amplifier should be designed so that the maximum input power is kept at 5 to 10 dB below the 1 dB gain compression point of the amplifier.

AM/PM conversion is a phenomenon wherein changes in the amplitude of the input signal applied to a non-linear circuit cause a phase shift. All amplifiers are essentially non-linear devices so all amplifiers will exhibit some degree of AM/PM conversion.

It is useful to note also that a linear bandpass filter can produce variations in the phase modulation at the output as a function of amplitude modulation on the input signal. This parameter is normally only of concern in power amplifiers or in systems using very complex modulation schemes, for example travelling wave tube amplifiers and 64 quadrature amplitude modulation respectively.

Amplifier gain is a factor is critically associated with bandwidth. As the bandwidth increases generally so does the noise figure. Gain figures typically ranging from less than 10 dB up to 62 dB are available either in single or cascaded stages. This parameter has to be selected with care to ensure optimum system performance in terms of intermodulation product generation, harmonic generation, noise figure and critically, automatic gain control considerations.

System design would identify the requirements of front end gain as an element in determining the system dynamic range. Post processing gain via a fast fourier transform processor will assist in deriving the actual system gain. More will be said about this later in the report.

Bipolar and FET amplifiers exhibit different overdrive response and recovery characteristics. When a bipolar amplifier is driven into compression or saturation, signal integrity will be lost because the high signal level changes the operating point of the transistor inducing bias circuit ringing. In those applications where pulse response and waveform integrity are important parameters, a bias circuit that does not employ reactive components can be utilized. FET amplifiers exhibit a generally superior saturation recovery capability because of their design. The system designer has to consider external circuitry when considering this parameter. Layout of the components and signal path lengths all contribute to the pulse recovery capability of the system.

Cascading individual amplifiers will influence the system recovery time as will the extent to which the input signal power level drives the system into saturation. The transient response of the system will dictate the degree of overshoot and ripple on the processed pulse, which would lead to amplitude distortion of the input signal. Recovery time can be as long as 5 usec and as has been indicated is very dependent on the input signal power. A more typical figure from manufacturers data provides for a recovery time of the order 1 to 3.5 µsec.

A measure of the power output capability of an amplifier is the 1 dB Gain Compression Point (GCP). This point is derived from a comparison of the input and output power levels of the amplifier. The difference between these levels is the gain of the amplifier and that point where the gain of the amplifier decreases by 1 dB is known as the 1 dB gain compression point. Either the input power or output power figures can be used to specify this point. An amplifier can be considered to still be in its linear region up to the 1 dB gain compression point but in a non-linear saturation region after this point. Typical power output figures for 1 dB GCP from various manufacturers data range from 0 dBm up to +25 dBm for medium power amplifiers. Typically high power amplifiers are not needed in receivers.

Whether the system designer selects a low noise amplifier or a high gain amplifier, the cost of the amplifier device itself is not considered excessive. Price breaks are offered by manufacturers depending on the quantity purchased. Given that a low number of devices are likely to be required, it is unlikely that any price break would be given and so the maximum price would be paid. Component costs are likely to range from $1.00 up to $50.00 or higher depending on the combination of amplifier parameters and the package and size considerations. Should the amplifier be required to meet military specifications, then the individual cost of this, and all other components for that matter, will likely be a factor of about four higher than the commercial part.

As a result of technology advancement and improvements in fabrication processes, reliability of electronic components has improved steadily over the years. As the amplifiers under consideration are pre-packaged and commonly hermetically sealed, reliability of commercial devices now approaches that previously restricted to military qualified products. Manufacturers are now often required to follow rigid quality control procedures starting from raw material procurement through product production and final inspection. Often, commercial components are manufactured to meet military standards but do not undergo formal military test procedures. The result of all this is that MTBF's of the order of thousands of hours are applicable to individual components.

Front end design layout constraints follow generally accepted analog layout procedures. Positioning of the components should be undertaken to ensure minimum signal path lengths. Shielded coaxial cable should be used for RF signal runs and separate voltage rails should be used to power the analog and digital circuitry. Ground returns are also a critical consideration to obtain minimal noise corruption and ensure good sensitivity for the receiver.

A choice of linear or switched mode power supply has to be made by the system designer. Each type has some advantages but the disadvantages should be carefully considered. The linear power supply will exhibit very low ripple on the voltage rails, of the order of 5 to 10 mV peak to peak. Compare this with a switched mode power supply exhibiting a peak to peak voltage ripple of the order of 300 mV, partially dependent on the current required. Certainly high on the advantages list of the switched mode approach is efficiency, size and weight. Switched mode systems exhibit efficiencies of the order of 75% to 80% if pulse width modulation is incorporated as a means to respond to current demand. They are significantly lighter than their linear counterpart but the switching frequency can become a source of spurious signal generation if sufficient decoupling is not included in the design. This is particularly true for maintaining receiver local oscillator purity.

2.1.2 Automatic Gain Control Considerations

The requirement for Automatic Gain Control (AGC) can easily be established to ensure maximum performance of the receiving system. Any amplitude modulation on the carrier signal should be retained and therefore linear amplification is essential. Loss of signal characteristics could lead to failure in identification and therefore reduce the performance of the system.

If an input signal is of a level that causes any amplification stage to saturate and therefore to become non-linear, then distortion results. Following stages are then subjected to harmonic and intermodulation products of true signals, as well as the true signals, and processing is adversely affected. Should the signal input level increase further, then the situation worsens and the signal information may become entirely unrecoverable. AGC offers a means of reducing or avoiding this situation and the following paragraphs review various means of implementing AGC.

2.1.2.1 Attenuation AGC

Figure 2.1.4 illustrates the basic concept of attenuation AGC. Here the attenuator is under voltage control and placed ahead of the amplifier chain to prevent the input signal from saturating the amplifiers. The AGC detector derives an output signal which is proportional to input signal strength, and feeds a differential amplifier. A reference voltage is also fed to the differential amplifier, the amplitude of which determines the operating point of the detector. The low pass filter is included for two prime reasons. The time constant of the low pass filter should be sufficiently long to prevent instability of the loop and the AGC

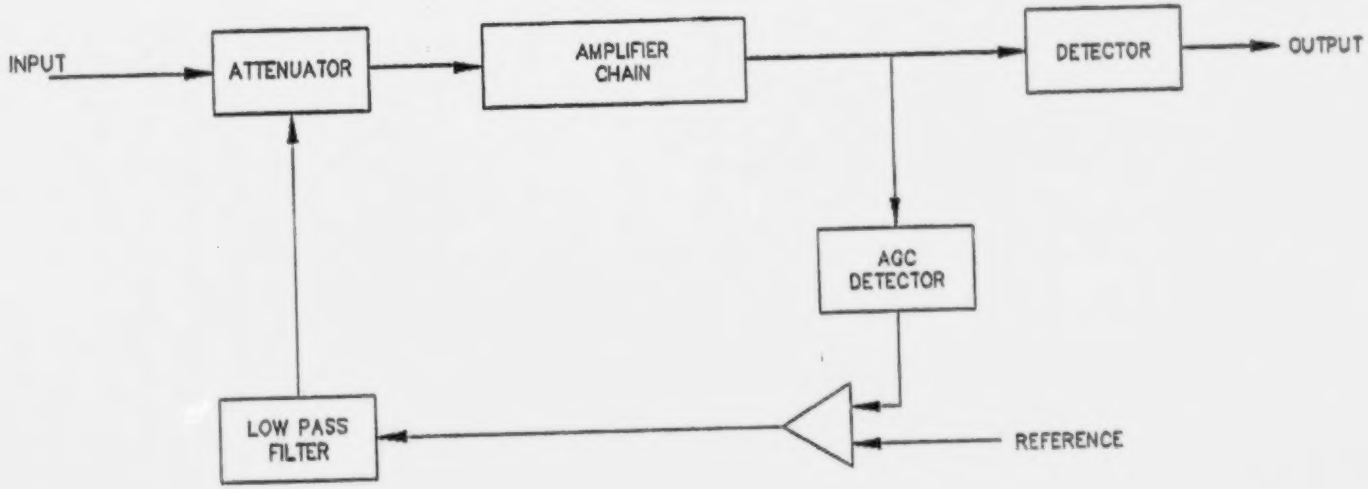


FIGURE 2.1.4 BASIC CONCEPT OF ATTENUATION AGC PROVIDED BY VOLTAGE VARIABLE ATTENUATORS

voltage must not be allowed to match low frequency modulation that could be present on the incoming signal. A design of this type would ensure that the input to the amplifier chain would be very nearly constant. How constant the actual signal becomes is dependent on the AGC loop gain, but provided the amplifier chain is prevented from entering saturation or going non-linear, the design would be acceptable.

For an improved front end layout of attenuation AGC, the attenuators should be distributed between the amplifiers. The main problem with the basic configuration shown in Figure 2.1.4 lies with the system signal to noise ratio (SNR). As the signal into the amplifier is effectively constant and the noise in the amplifier is constant, so the output SNR is constant, regardless of signal strength. By distribution of the attenuation, the overall noise figure for the system can be buffered by the amplifiers and restricted to a lower figure than would be the case with lumped attenuation. The improved configuration is illustrated in Figure 2.1.5.

In practice, the lowest noise performance is obtained by applying attenuation closest to the output first and gradually applying attenuation back towards the input. To accomplish this, delay has to be introduced to the earlier attenuator control signals to maintain the lowest system noise figure and prevention of compression of any stage. For an improvement in system response time, the system should provide proportional attenuation to all the amplifiers in the chain thereby maintaining the fastest response time.

Design of the low pass filter illustrated in Figures 2.1.4 and 2.1.5 determines the pulse response time characteristics of the receiver. A conventional RC low pass filter would provide a time constant attack/decay characteristic while a dual time constant low pass filter (where the charge time is less than the discharge time) will provide a fast attack, slow decay AGC. The

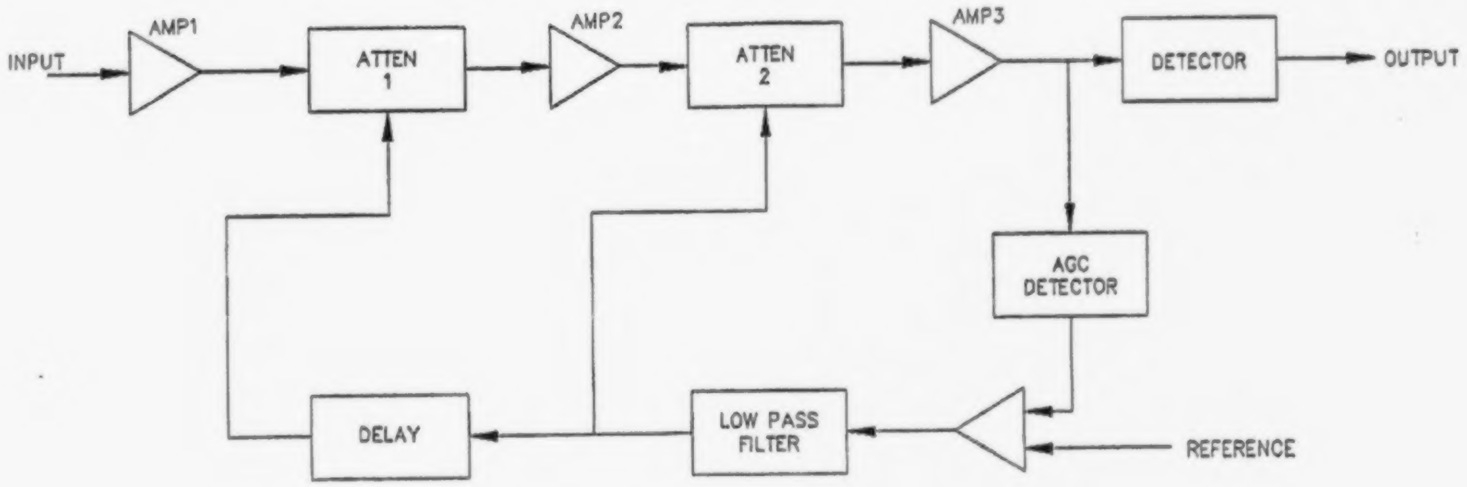


FIGURE 2.1.5 DISTRIBUTED ATTENUATOR CONCEPT OF ATTENUATION AGC PROVIDED BY VOLTAGE VARIABLE ATTENUATORS

selection of the attack time constant is based on ensuring that any modulation information in the original signal does not appear in the AGC loop. If any low frequency modulation appears in the AGC control loop then corruption or elimination of the input signal at the receiver output could result. This approach tends towards a peak level detection of the input signal and therefore this form of AGC is amplitude modulation dependent. For suppressed carrier systems where energy exists only in the sidebands, the fast attack, slow delay type of AGC is essential for the recovery of the encoded signal.

2.1.2.2 Variable Gain Amplifiers

This type of gain control consists of altering the actual gain of the amplifier in proportion to the signal fed from the detector. Various methods can be used to achieve this objective. The amplifier gain can be altered by changing the transistor operating point or more preferable by altering the gain of the stage and not changing the transistor operating point. Altering the transistor operating point has disadvantages of altering the transistor dynamic range and that the transistor frequency characteristics are altered.

Diodes placed in the emitter or collector legs of the transistor can be used to alter the circuit gain without affecting the transistor itself. Additionally, the transfer function can be controlled by this method. FET transistors can also be used as a frequency insensitive variable attenuator responding to voltage control within a monolithic package. Use of these techniques has to be carefully considered in terms of their temperature effects.

Variable gain amplifiers can respond to control voltage inputs quite rapidly, typically less than 10 usec. Control voltages can be digitally controlled if desirable and typically range between 0 to +5 volts or 0 to +10 volts. With a 0 volt control voltage level, the amplifier exhibits maximum gain and as the control voltage increases so the amplifier gain decreases. Devices of this type present an increase in noise figure as the control voltage increases but the increase is typically around 25%. This does not present a major problem for the designer because although the system noise figure will increase and system sensitivity worsen, the amplitude of the input signal would be sufficiently high that an acceptable signal to noise ratio remains.

2.1.2.3 Switched Gain Amplifiers

Under an instruction derived from the output level of the detector, the gain of the amplifier would be selected from a number of alternatives and switched into circuit. This form of AGC is dependent on the time required for the switching circuit, and there are devices available that can switch very fast and these devices provide for a very fast gain change. The essential problem with this technique is that only discrete levels of gain are available. A potential problem arises when the signal level during the received pulse increases beyond the threshold of gain change and therefore forces a re-selection of circuit gain. The system design would have to allow for this eventuality and prevent a gain change during the reception of a signal, as information may be lost during the switching process.

2.1.2.4 Logarithmic IF Amplifiers

For an amplitude measurement system, a logarithmic amplifier can be used as a means to input an RF signal and output a log video signal. The video output represents the log of the input signal and the amplifier can provide RF gain and improve sensitivity and dynamic range of the receiver. In a practical receiver design, both a linear and logarithmic channel would exist.

An IF log video amplifier generally comprises several stages of cascaded amplification with a detector at the output of each amplifier as shown in Figure 2.1.6. The outputs from the detectors

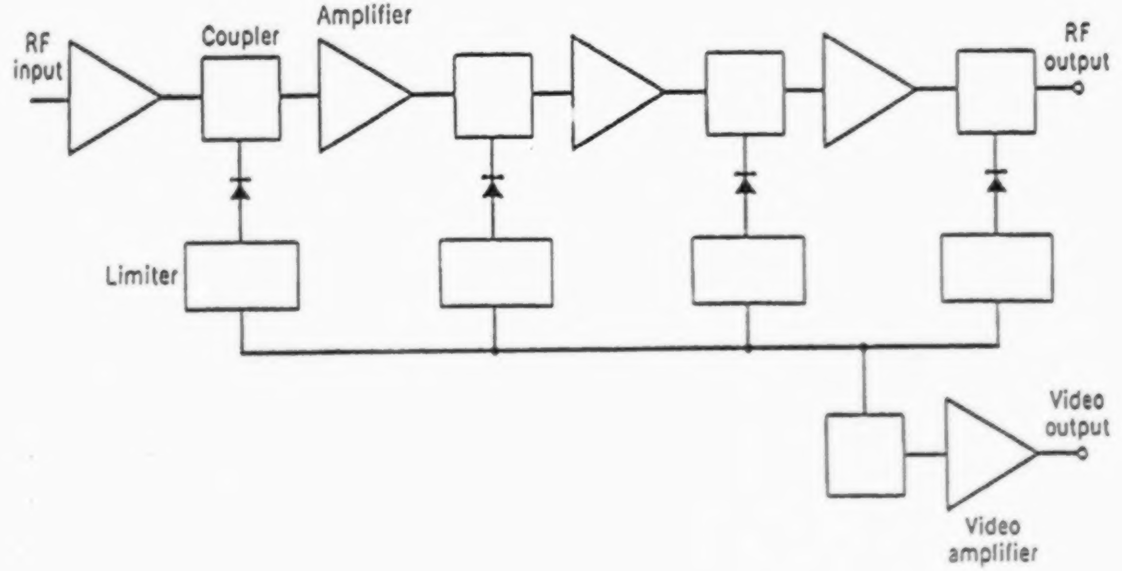


FIGURE 2.1.6 AN n STAGE SUCCESSIVE DETECTION RF LOG AMPLIFIER

are amplified and summed in a log circuit. In Figure 2.1.6, video limiters are included to eliminate the constraint of designing an RF amplifier stage with controlled limiting characteristics while maintaining the desired linear response. Video limiting begins while the RF amplifier is still operating in the linear region.

The output from the summing circuit is proportional to the log of the power of the RF input signal. A weak input signal is amplified through the chain of amplifiers and detected by the last few detectors, while a strong signal would be detected by all the detectors. Dynamic range of such a receiver can be improved with this design as each detector only covers a portion of the RF range. A dynamic range in excess of 85 dB can be achieved using this approach.

Each amplifier in Figure 2.1.6 has to compensate for the coupling energy lost to the detector and the amplifier must contain sufficient stages to provide the desired dynamic range. A different delay time should be introduced at the output of each detector such that the video signals arriving at the video amplifier are time coincident. This is required because of the finite delay between the RF amplifier outputs.

Response time of an IF amplifier is of some concern depending on the particular application. Generally, the rise time is short while the trailing (fall) time is relatively long, but using detectors with smaller parasitic capacitance may shorten the trailing time. The video amplifier can be AC or DC coupled where AC coupling allows amplitude measurement of pulsed signals and DC coupling allows amplitude measurement of both pulsed and CW signals. One disadvantage of using DC coupling is that the baseline may drift and readjustment of the output level may be required.

Due to the logarithmic nature of the amplifier, the rise time of a pulse should not be taken to be the conventional 10% to 90%

definition. A more appropriate definition would be the minimum input pulse width for a 1 dB error. This definition provides for the case where the rise time may be 50 nsec for example, but it may take 125 nsec to settle to within 1 dB of the final value. This time would be input signal level dependent. With current integrated circuit techniques, devices are readily available having excellent pulse responses and recovery times of less than 200 nsec. Such devices can amplify pulses having widths of the order of 20 nsec.

2.1.2.5 Tuneable Bandpass Filters

A method of protecting a receiver against higher power input signals that force the system AGC to react and potentially nullify the lower power signals is to incorporate a tuneable bandpass filter. In such a situation, the bandpass filter can be aligned to those parts of the spectrum outside the higher power signal and thereby effectively select the signals of interest. Given this situation, the receiver can be permitted to operate with a lower input signal level and continuously in the linear range minimising spurious intermodulation and harmonic signals. This provides for a lower system noise figure and improved response time as the receiver remains out of saturation.

On the down side, the probability of interception diminishes as only part of the relevant spectrum is covered and this may become a significant problem if the input signal is frequency hopping. The bandwidth and out of band attenuation of the band pass filter become critical parameters in terms of the overall system design.

The bandpass filter should be tracked along with the LO signal thereby ensuring that the signal of interest is appropriately down converted to the IF circuitry. The tuning rate of the bandpass filter has to be selected to be able to track the frequency hopping radios that the system is expected to follow. More data would be required to permit a more detailed analysis of this problem to be discussed further.

2.1.2.6 Tuneable Notch Filters

Similar to the approach discussed in the previous section, this approach effectively removes any high power signal thereby allowing lower power signals to be processed. The notch filter would be narrowband and have a depth of attenuation much greater than would be derived from the bandpass filter attenuation characteristic.

A review of the relevant spectrum would be required in order to determine where the notch filter(s) should be placed and some method of periodic look through would also be required to determine whether the offending signal is still transmitting. The tuning rate of the notch filter would dictate how quickly an offending signal can be removed. This technique would permit lower power signals to be processed, thereby allowing the optimised use of the system AGC.

2.2 Analog to Digital Conversion

Analog to Digital conversion techniques are described in this report fall into two major categories; single channel A/D's and parallel sampling A/D's. The first category, single channel A/D's includes six different architectures which are in common use today and are discussed in Sections 2.2.1 to 2.2.3. The second category, the parallel sampled A/D converter includes two recently developed architectures and is discussed in Section 2.2.4. A number of performance parameters and definitions are used to compare the various technologies. Should the reader not be familiar with these terms, several appendices have been included to assist in the interpretation of this report, see Appendices B, C, D and E.

2.2.1 Flash A/D Converters

As the name implies this is the fastest Analog to Digital converter available on the market today. The parallel architecture for an n-bit flash converter consists of 2^n-1 comparators connected in a ladder fashion as shown in Figure 2.2.1. The output of the comparators are fed to a 2^n to n bit encoder whose output is latched and buffered. The speed of such an architecture is determined only by the sum of propagation delays of the comparators, the encoder and latching logic. With current state-of-the-art we can find flash converters operating at above 300 MSPS for 8 bits of quantization, and 10 bits at 20 MSPS.

In reality this architecture has a major drawback, in that, if we want to add an extra bit of quantization, we must double the number of comparators. This is one reason why we do not see A/D converters with more than 10 bits with the present level of technology and another is because the input capacitance is proportional to 2^n. Therefore, in the near future will we see "flash" converters becoming faster, but it will take some time before the quantization level expands to more than 10 bits.

Another problem associated with flash converters is the power dissipated. High speed ECL logic is used to implement most of the flash architecture, therefore, the power consumed by these devices exceeds the power dissipated by other types of architectures of A/D converters.

The flash approach is also characterized by a high input capacitance. From Figure 2.2.1 we see that the input voltage Vin sees a total input impedance:

$$Zin = Rin \mathbin{//} [2^n-1]\, C_{comp} \qquad \text{eq. (3)}$$

As we are going to see later in Section 2.2.4.2.3, this input capacitance is going to degrade the "input bandwidth" frequency

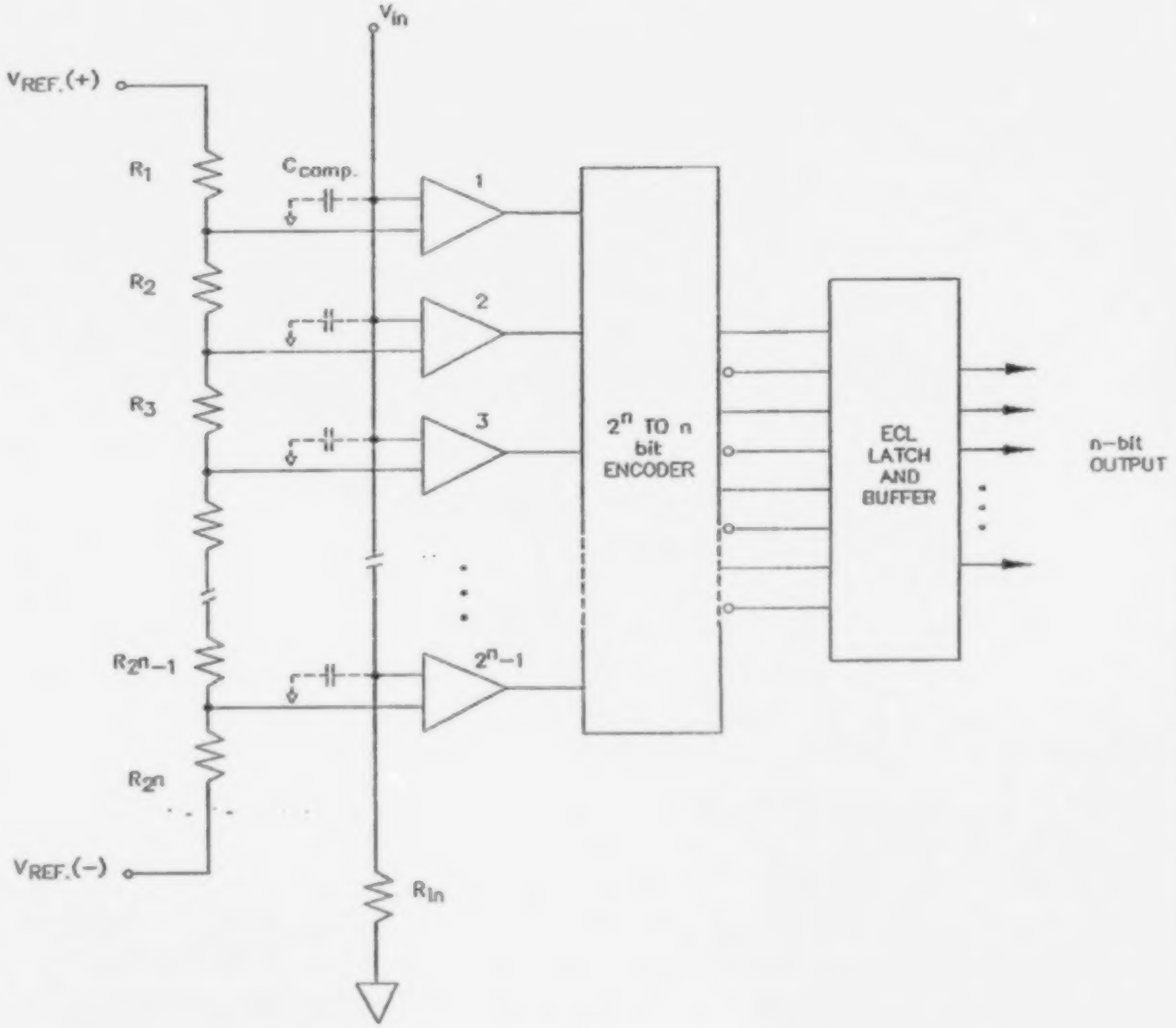


FIGURE 2.2.1 TYPICAL ARCHITECTURE OF A FLASH CONVERTER

response, unless the manufacturer is able to keep C_{comp} to a reasonable value.

The accuracy of flash converters is limited by the offset and hysteresis of the comparator technology being used. With today's technology we find flash A/D converters with ± 1/2 LSB integral linearity and ± 1/2 LSB of differential linearity over the full scale range (FSR).

The linearity problem can be improved in flash A/D converters since we have direct access through some "taps" on the quantization chain of resistors which is characteristic of these types of converters, see Figure 2.2.1.

By connecting appropriate external circuitry to a flash A/D converter, Figure 2.2.2, we can improve the linearity transfer function as shown by Figures 2.2.3(a) and (b).

Flash converters require an external reference source which supplies the quantization chain of resistors. This reference source must be very stable or serious linearity problems can occur.

Finally, we must look at the input and output considerations of flash converters. The logic used in high speed flash converters is ECL logic and as a result the input voltage range most commonly found is from 0 volts to -2.0 volts.

The output of the flash converters is normally differential ECL logic, with output coding based on either "straight binary" or "inverse binary" which can be easily converted to a two's complement by inverting the most significant bit (MSB). Some converters have programmable output coding which the designer selects depending on the application.

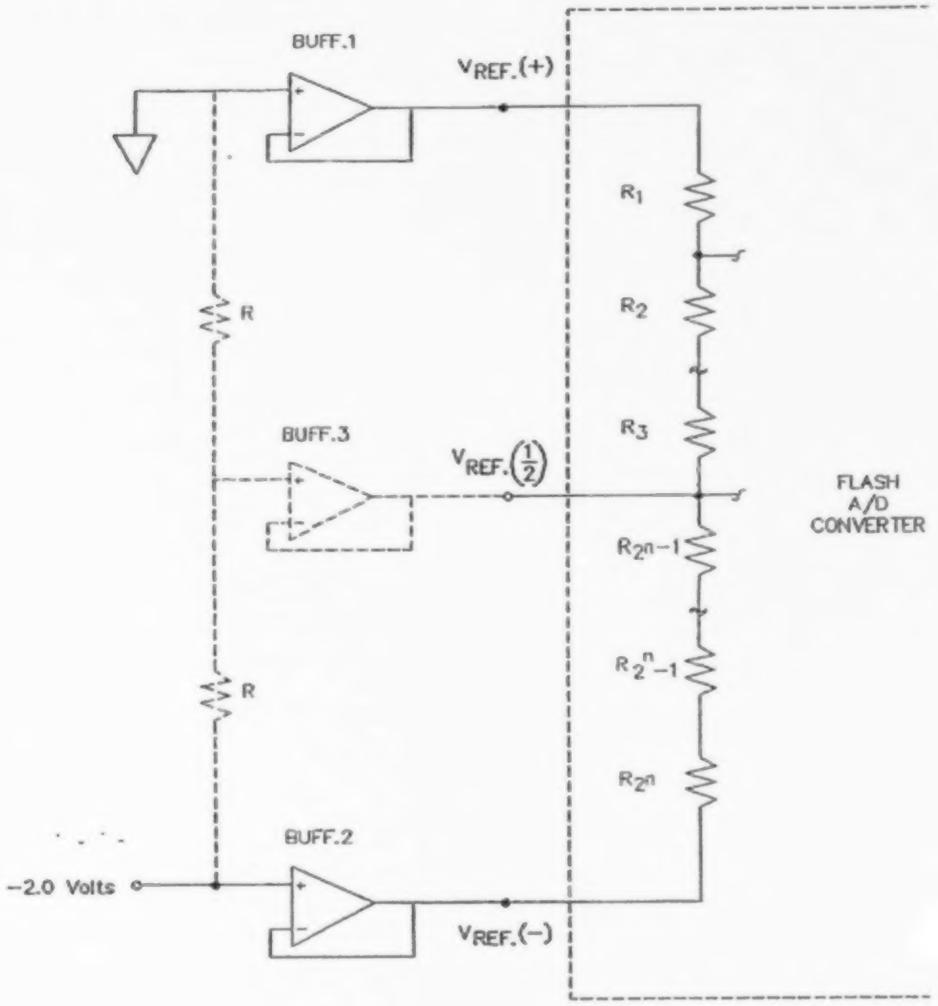
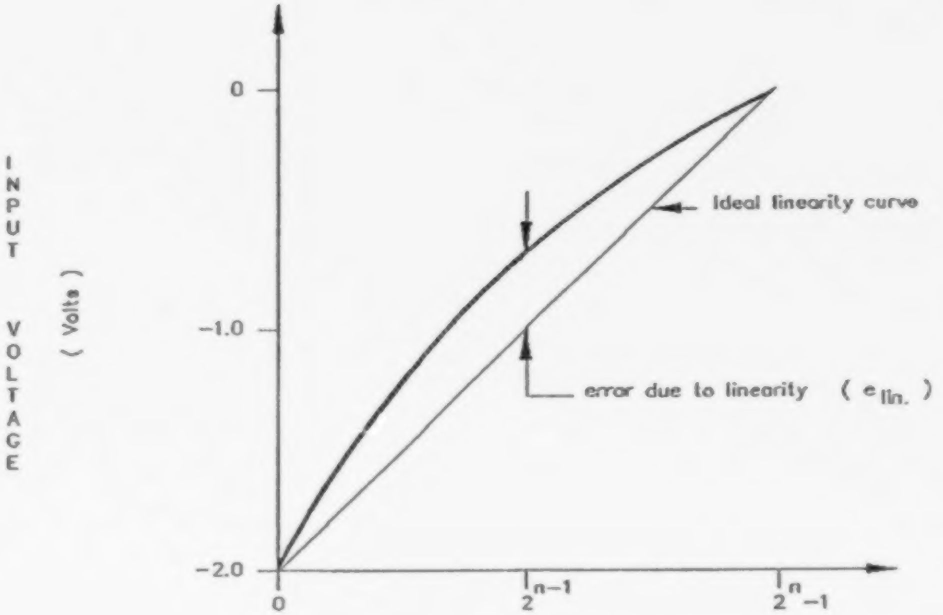
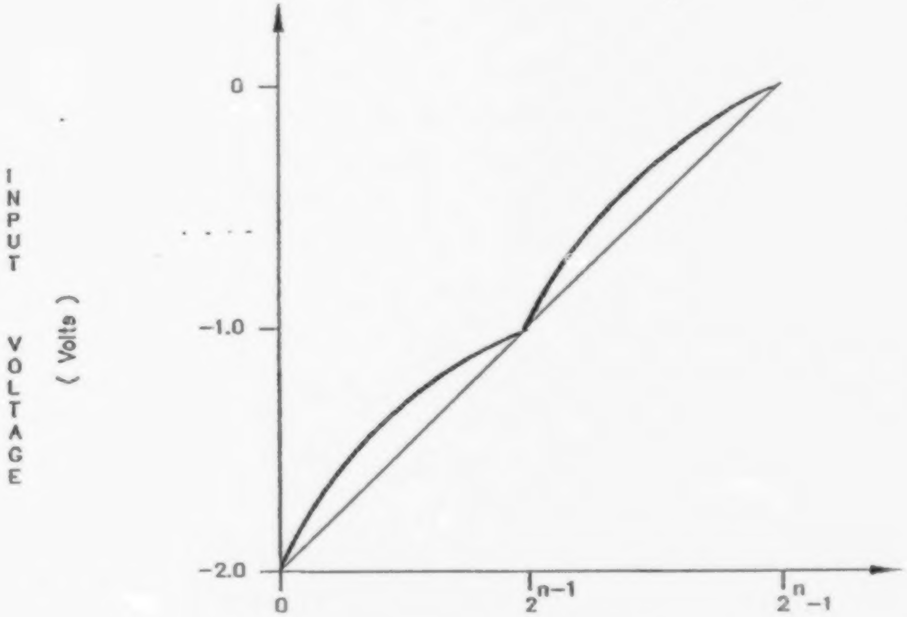


FIGURE 2.2.2 IMPROVING THE LINEARITY TRANSFER FUNCTION BY ADDING (BUFF.3) (SEE FIGURE 2.2.3 a,b)



BIT NUMBER

FIGURE 2.2.3(a) LINEARITY CURVE WITH NO TAP ADJUSTMENT



BIT NUMBER

FIGURE 2.2.3(b) LINEARITY CURVE WITH TAPS FORCED TO $\left[\frac{2}{5} e_{\text{LIN.}}\right]$ BY USING BUFF.3

2.2.2 Feedback A/D Converters

A typical feedback A/D converter is shown in Figure 2.2.4. The most common feedback A/D algorithm is the "successive approximation" or series-feedback algorithm. This approach uses a single bit comparator and requires one clock cycle per bit of conversion plus one or more additional cycles to allow for acquisition and settling time of the sample and hold (S/H). The actual maximum clock speed is limited by the time for the feedback circuit to respond to the error signal. Therefore the maximum sampling rate is given by:

$$\text{fsamp.}_{(MAX)} = \frac{\text{fCLOCK}_{(MAX)}}{n} \qquad \text{eq. (4)}$$

where n = number of bits
fsamp = ext. sampling pulse
fCLOCK = int. clock frequency

The conversion rate of a feedback A/D can be increased by using more than one comparator in the quantizer to determine more than one bit per clock cycle, thereby requiring fewer cycles to complete the conversion. This architecture is called series-parallel feedback (Figure 2.2.4(c)) and is capable of higher conversion rates at an increase in A/D complexity. The number of contributors to A/D nonlinearity error increases considerably over the successive approximation algorithm.

A third version of a feedback A/D is the series-parallel subranging algorithm which is shown in Figure 2.2.4 (b). This architecture is a little faster than the series-feedback and less complex than the series-parallel architecture. The subranging technique uses two or more passes to obtain the final conversion for an input signal. Because there are three different versions of the architecture for the feedback A/D, we find that there is a wide variety of conversion speeds and quantization resolutions for

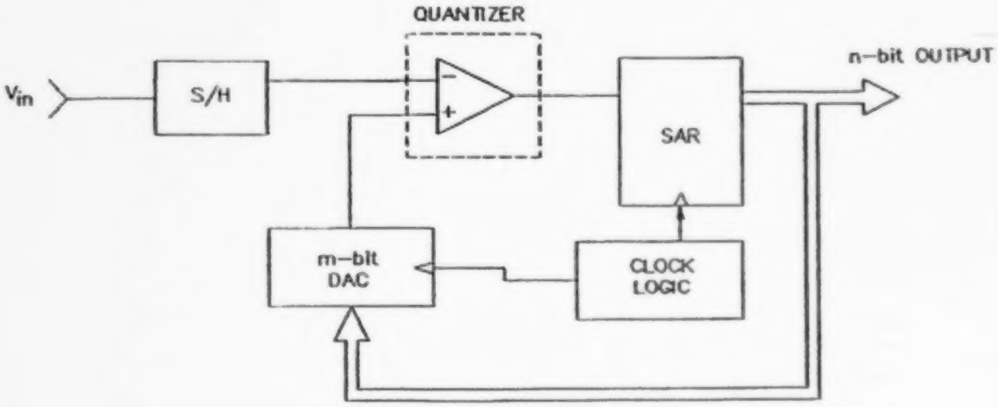


FIGURE 2.2.4(a) SUCCESSIVE APPROXIMATION OR SERIES-FEEDBACK A/D CONVERTER

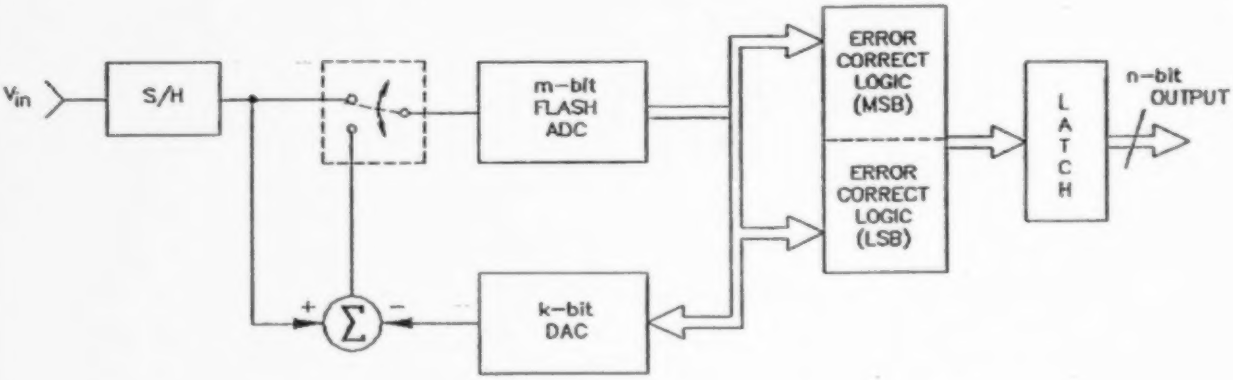


FIGURE 2.2.4(b) SERIES-PARALLEL FEEDBACK (SUBRANGING TECHNIQUE) A/D CONVERTER

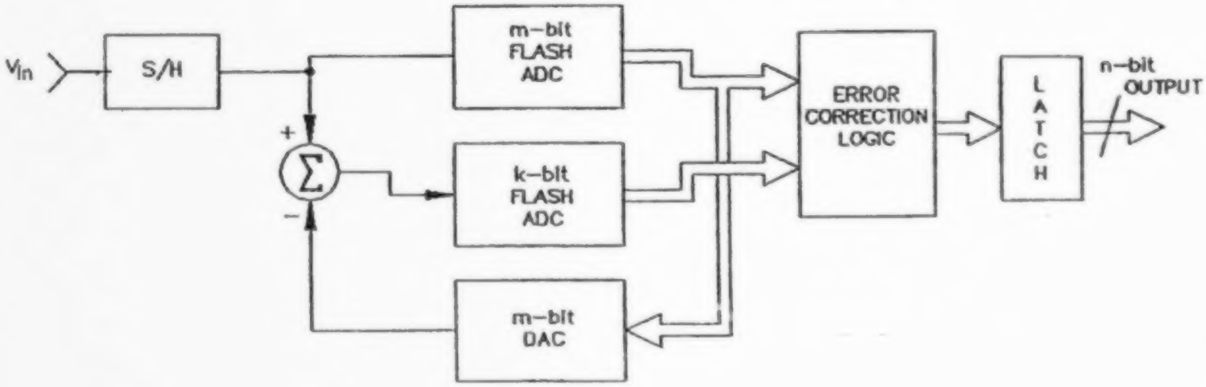


FIGURE 2.2.4(c) SERIES-PARALLEL FEEDBACK A/D CONVERTER

A/D's based on this particular architecture. As an example we have A/D's that convert signals at 400 KHz with 16 bits of quantization and 20 MHz with 12 bits of quantization.

The fastest successive approximation A/D's use their internal clock to step through the conversion mechanism once an external sampling pulse is given to the device; this is to ensure that the high speed performance is kept.

The power dissipated by the A/D based on the feedback architecture depends on which version of the algorithm is used. From a survey of the technology on these types of A/D, the successive approximation algorithm using a single comparator and a successive approximation register (SAR) is based on CMOS technology, therefore power dissipation in these converters is very small.

The quantizer on the subranging series-parallel and series-parallel A/D converter is based on low resolution flash converters, therefore ECL logic is used to achieve the higher throughput rates, consequently the power dissipation increases accordingly. Table 2.2.1 illustrates a typical relative power for each of the architectures described so far.

For proper operation, the feedback architecture requires a sample and hold amplifier at its input. Some manufacturers include a S/H device in the same A/D package which will ease the interface of the digitizer to the rest of the circuit. If an input S/H is not included in the architecture of the A/D then a selection must be made according to the required application (see Section 2.2.5).

Architecture	Power
Flash	High
Series-Parallel Feedback	Medium to High
Subranging Series Parallel Feedback	Medium
Successive Approximation	Very Low
Feed Forward	High

Table 2.2.1 Comparison of Power Requirements for Various Types of A/D Converter Architecture.

The input impedance of the feedback architecture is dependent only on the input capacitance of the amplifier-comparator circuit in the case of the successive approximation A/D or the input impedance of the sample and hold amplifier. There is a wide range of input impedances depending on the type of algorithm implemented in the design and also on the technology used by a particular manufacturer..

Generally, feedback architectures have internal references and input buffers with programmable input voltage ranges so that application of the converter is made much simpler from the designer point of view.

Integral and differential linearity are comparable to the flash architecture except when A/D's have a high quantization resolution such as a 16 bit A/D using successive approximation might have linearity equivalent to a 14 bit A/D. This is due to the wide dynamic range required by the comparator input circuit.

Because of the lower conversion speeds, the output of the feedback architecture is normally based on TTL logic with a variety of output coding.

2.2.3 Feedforward A/D Converters

The highest performance A/D architectures are feed-forward or pipeline algorithms. A general block diagram of a feed-forward A/D is shown in Figure 2.2.5. The algorithm consists of a succession of quantizer/subtractor stages, each of which determines one or more bits of the conversion and passes a residue analog signal on the next stage. The inclusion of a S/H or some other means of analog delay in each stage allows all stages to simultaneously determine their assigned bits for successive samples of the analog input. The simplest version is the series feedforward architecture which determines a single bit per stage. This approach uses a S/H and a comparator in each of N stages for an N bit conversion.

The series feedforward or series-parallel feedforward architecture is useful for 6 to 12 bit range A/D converters. The conversion speed achieved with current state-of-the-art is in the neighbourhood of 10 MHz to 20MHz such as the Burr-Brown A/D-603 12 bits at 10MSPS. The feedforward architecture is very similar to the series-feedback in terms of input parameters, i.e. impedance, input voltage range and power dissipation.

The major problem with this architecture is the high number of error sources introduced on the residue as it is fed from one stage to the next. As a result, all manufacturers using feedforward architectures use only a single quantizer/subtractor stage to keep the error within acceptable limits.

The outputs of the feedforward architecture use differential ECL logic due to the higher conversion rates. Different output

NOTE: FOR SERIES–FEEDFORWARD
REPLACE EACH FLASH CONVERTER
BY A SINGLE COMPARATOR

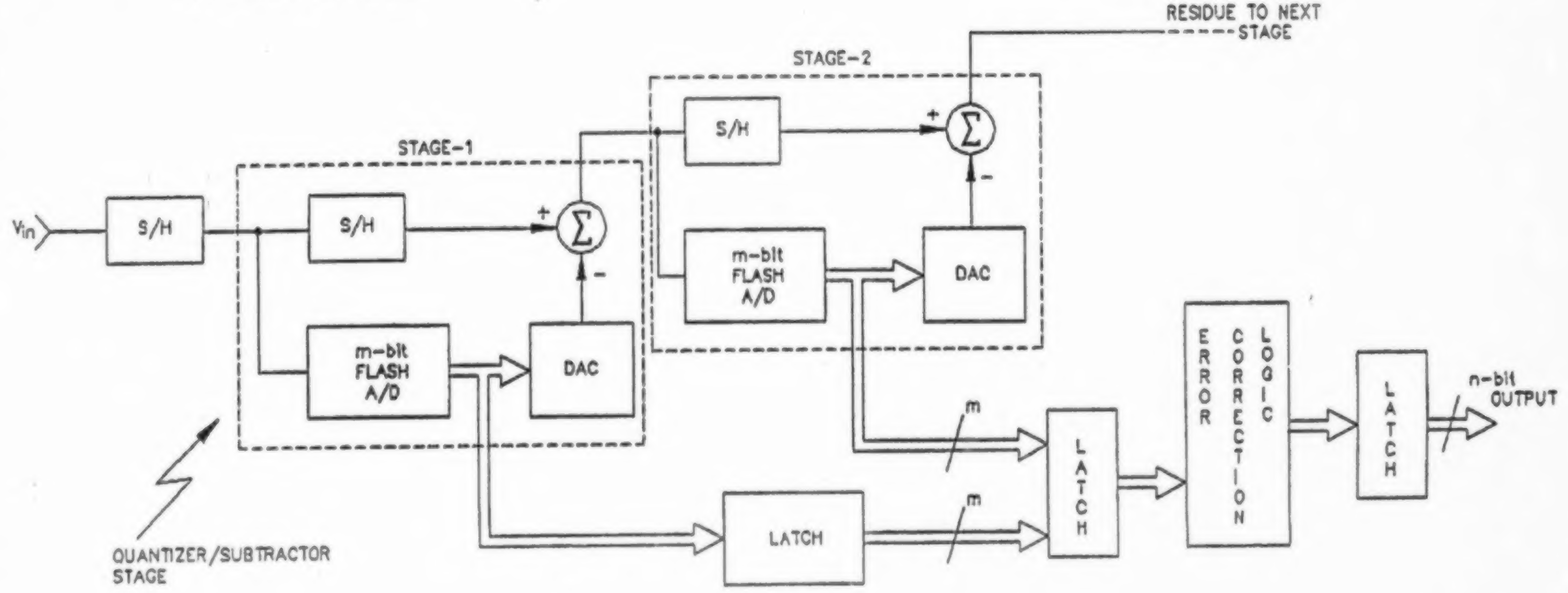


FIGURE 2.2.5 SERIES–PARALLEL FEEDFORWARD
A/D CONVERTER

codes are available and most manufacturers provide output code programming in order to suit different applications.

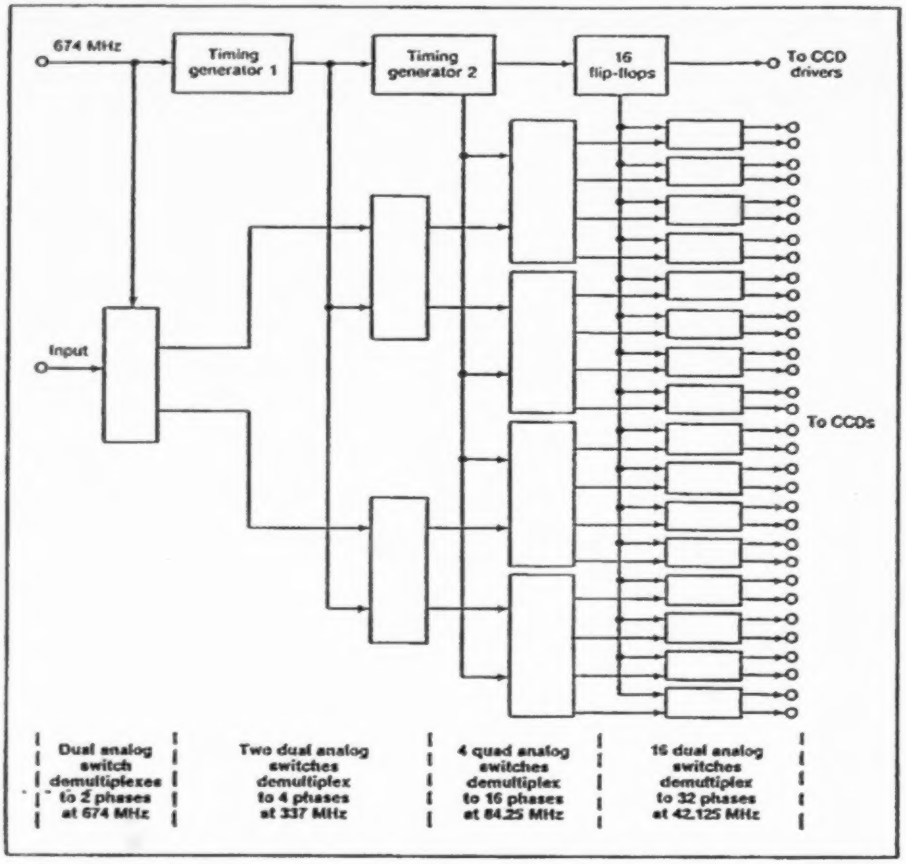
2.2.4 Parallel Sampled A/D Converters

2.2.4.1 Fast-In Slow-Out

There exist many permutations to the parallel sampled A/D converter. Two basic approaches are currently being offered in the commercial market place.

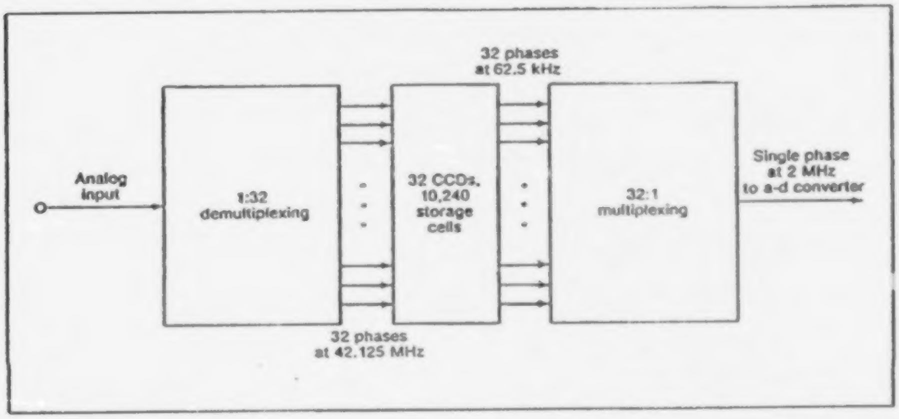
The first of these methods is characterized by a fast input but a slow output of data. One version of the method, shown in Figure 2.2.6, utilizes four stages of analog demultiplexers to generate 32 phases of analog output at 1/32 the 1.3 GSPS input rate. This system relies on a first stage 1P2T switch to demultiplex the input signal into two analog samples, one directed to each output. After this is achieved, slower analog switches are used to further demultiplex the analog samples into 32 parallel analog outputs. The net effect is the realization of a 1P32T switch with a 380 psec aperture.

This system, shown in Figure 2.2.7, then passes the 32, 380 psec wide analog samples to 32 parallel buffer amplifiers which in turn each drive a charge coupled device (CCD). The CCD's, each 320 cells long, are then clocked every 23.7 nsec, and are filled in 7.596 μsec. Once the CCD's are full they are output at a 16 usec clock rate through 3 stages of analog multiplexers to a single analog channel. The pulses then 0.5 usec apart are digitized by a single standard 12 bit A/D converter. This last stage requires 5.13 msec to quantize the 7.4 μsec sample. Hence the description, fast-in slow-out. Obviously this type of A/D converter is only useful for short sample lengths and cannot handle continuous digitizing of real-time signals.


674 MHz
Timing generator 1
Timing generator 2
16 flip-flops
To CCD drivers
Input
To CCDs
Dual analog switch demultiplexes to 2 phases at 674 MHz
Two dual analog switches demultiplex to 4 phases at 337 MHz
4 quad analog switches demultiplex to 16 phases at 84.25 MHz
16 dual analog switches demultiplex to 32 phases at 42.125 MHz

Demultiplexing is accomplished in four stages by banks of analog switches. Two timing generators operating at 674 MHz and 337 MHz sequence the operation.

FIGURE 2.2.6 FISO DEMULTIPLEXER



By demultiplexing the input signal at high speed into a bank of 32 CCDs, and multiplexing it back out at a much lower rate, the 6880 waveform digitizer samples at 1.348 gigasamples/s, yet its a-d converter only needs to work at 2 megasamples/s.

FIGURE 2.2.7 FISO SYSTEM (made by LECROY mod.6880B)

Some interesting comments can be made about the bandwidth of the FISO system.

The advertised system shown in Figure 2.2.7 has a Nyquist frequency, $0.5 \times f_s$, of 1.3 GSPS, which implies each of the initial channel samples is taken every 1.53 nsec. The system claims a 3 dB input bandwidth of 250 MHz, which, strictly from an aperture width point of view, would imply the sample widths to each channel are 1.76 nsec (see Appendices B and C, $1/.44\ t_a$ = 3 dB bandwidth). The actual sample aperture width is not advertised, but, if the first stage switch is assumed to operate on a 50% duty cycle, then the theoretical 3 dB bandwidth would be 1.14 GHz. It would appear that other factors such as parasitic capacitance must be seriously degrading the bandwidth response of this device.

One design trade off inherent with this type of fast-in slow-out A/D converter is that the required narrow pulse analog samples, in this example about 350 psec wide, and up to 1 Volt in amplitude do not represent a lot of charge for a sample and hold amplifier or CCD to work with. As a result, the total length of time required to hold this charge in the CCD has a direct effect on the amount of leakage and noise which will corrupt the small analog sample. A trade-off must therefore be made between the size of the analog charge stored in the CCD, the amount of time required to maintain the analog signal in the CCD memory, and the clock rate of the CCD. The total time the last sampled data point must be stored in analog form is approximately equal to $n/f_{A/D}$ where n is the number of samples taken and $f_{A/D}$ is the sampling frequency of the output A/D.

The number of CCD channels is dictated by the maximum clock rate of the CCD's and the total record length required. The total memory length, nf_s, must equal the number of CCD channels multiplied by the CCD length.

2.2.4.2 Fast In Fast Out

TELEMUS has developed a unique parallel processing architecture which allows the synthesis of a very high sampling rate Analog to Digital Converter system through the simultaneous use of multiple conventional A/D converters operated in parallel. The parallel technique permits the realization of systems with far greater sampling rates than can be currently achieved with single state-of-the-art Analog to Digital converters. The realization of such a system requires a number of component parts where each must operate successfully to achieve the ultra high sampling rates. The primary components of the TELEMUS A/D converter system shown in Figure 2.2.8 include the front end demultiplexer (demux), the high speed sample and hold amplifiers (S/H), the parallel flash converters and high speed memory architecture.

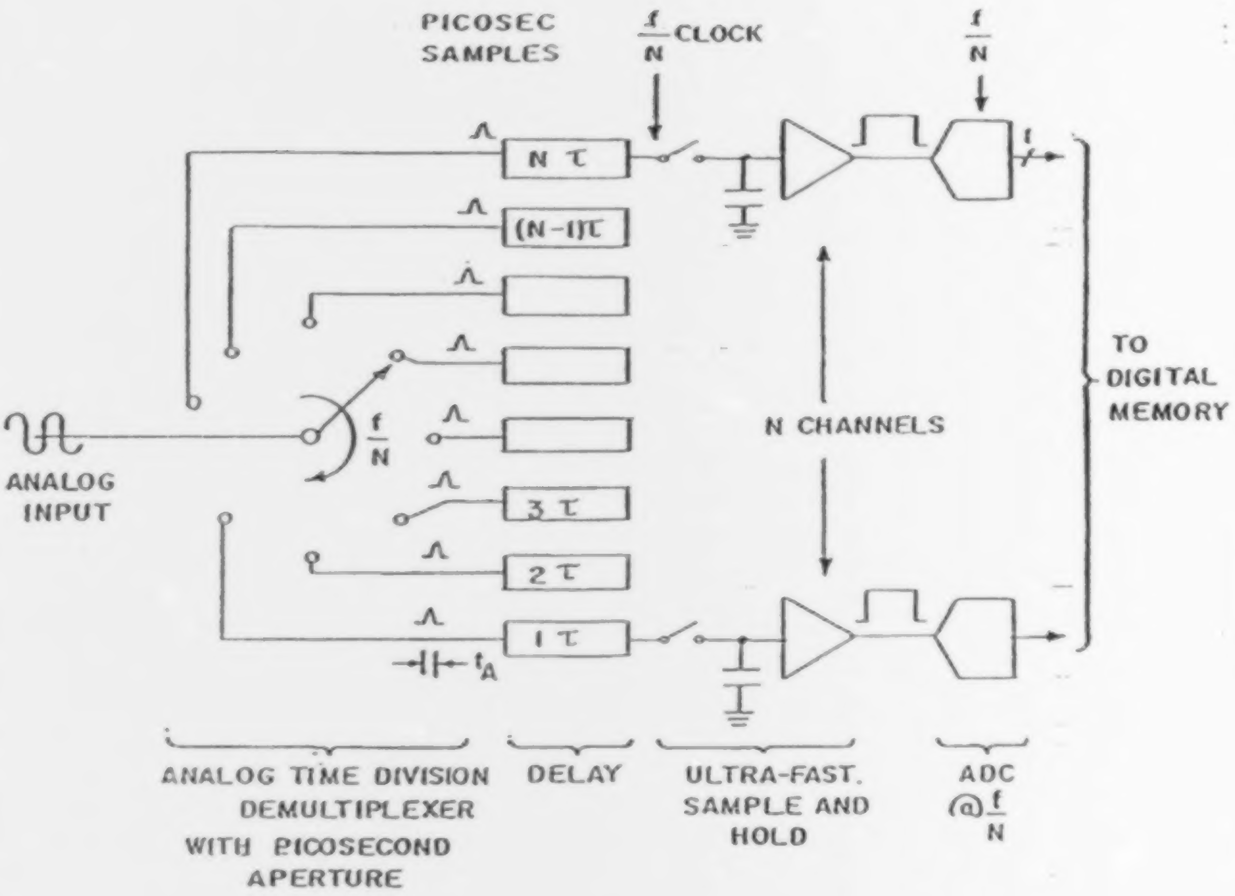
2.2.4.2.1 Parallel A/D Sampling Rate

The A/D converter System has a total sampling rate equal to the sum of the sampling rates of all the N channels. Hence if the system sampling rate is f_s Mega Samples Per Sec (MSPS) then each channel must run at f_s/N MSPS.

2.2.4.2.2 Parallel A/D Aperture Width

The length of time that the aperture is open at each channel of the parallel A/D, ie, the aperture width of the demultiplexer (demux) t_a, must be much less than $T_s = 1/f_s$ (see Appendix C).

The short aperture time of the demux results in a sampled analog pulse, t_a seconds wide. Since the parallel channels are sequentially sampled, the N sampled analog pulses must be aligned to arrive at the N sample and hold amplifiers simultaneously. The sample and hold (S/H) amplifiers are timed such that all N pulse samples are captured simultaneously. The S/H amplifiers then produce an output voltage proportional to the peak voltage of the



SAMPLE RATE f Mega Samples/Sec

N CHANNEL ADC SYSTEM

ADC CLOCK RATE f/N Mega Samples/Sec

FIGURE 2.2.8 THE FIFO ARCHITECTURE OF THE TELEMUS A/D CONVERTER SYSTEM

input sample pulse and hold that voltage constant for f_s/N seconds. The held output of the S/H amplifiers are then presented to high-speed flash Analog to Digital Converters. The flash converters sample the input signal every f_s/N seconds, thus digitizing every sample presented to them. The digital information is then passed to a high speed memory. The beauty of this technique is that both the aperture width and the aperture jitter of the flash converters is no longer critical so long as the flash converter aperture is opened while the S/H amplifier output is stable. The onus for stable aperture timing is completely placed upon the demux circuitry.

2.2.4.2.3 Parallel A/D Input Impedance

The input demux has another major advantage over a single channel flash converter architecture, that is its input impedance. A major problem with flash converters is their high input capacitance. The capacitance results from the 2^n-1 parallel comparators required to make up an n bit flash converter. For example an 8 bit flash converter has 255 comparators shunted across the input to ground. This creates a very low and complex impedance to the RF input signal. A typical 8 bit flash converter has an input impedance of 1KOhm//56pf.

Typically flash converters are used in parallel with a 50 Ohm load resistor to improve input match. The circuit model of such a circuit is shown in Figure 2.2.9(a). The input response of such a flash converter in a 50 Ohm system is shown in Figure 2.2.10. The input response was calculated for five different input capacitances in parallel with a constant 1KOhm input resistance and a 50 Ohm load resistance. The input response -3dB bandwidth represents the 70% voltage point, which in turn means a reduction in the effective number of bits, n_{eff}, by the following equation:

$$n_{eff\ 3dB} = n - 0.5 \text{ bits} \qquad \text{eq. (5)}$$

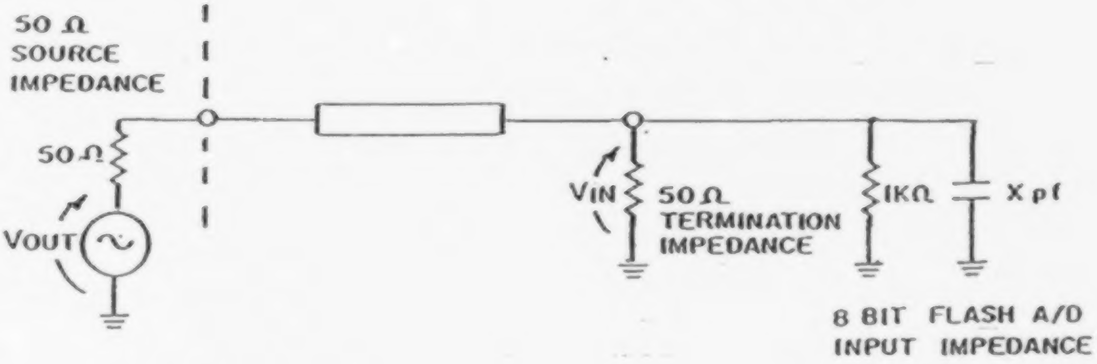


FIGURE 2.2.9 a) FLASH A/D IN A 50 OHM SYSTEM

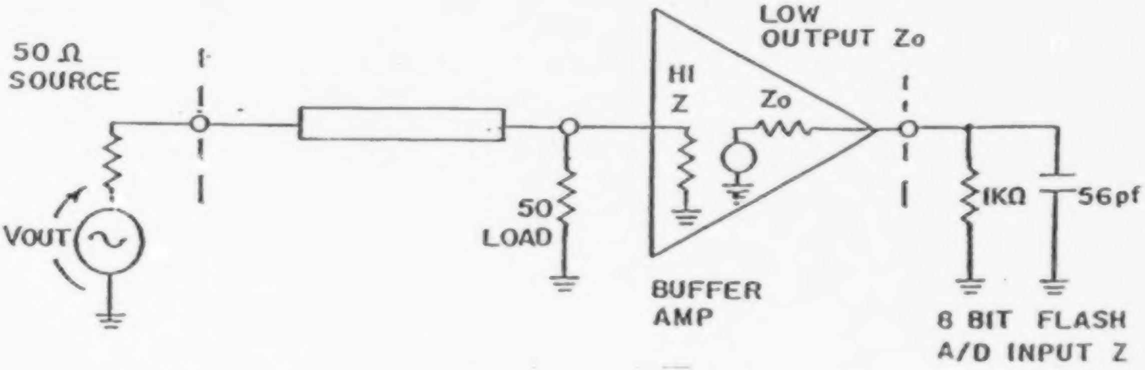


FIGURE 2.2.9 b) FLASH A/D WITH BUFFER AMPLIFIER

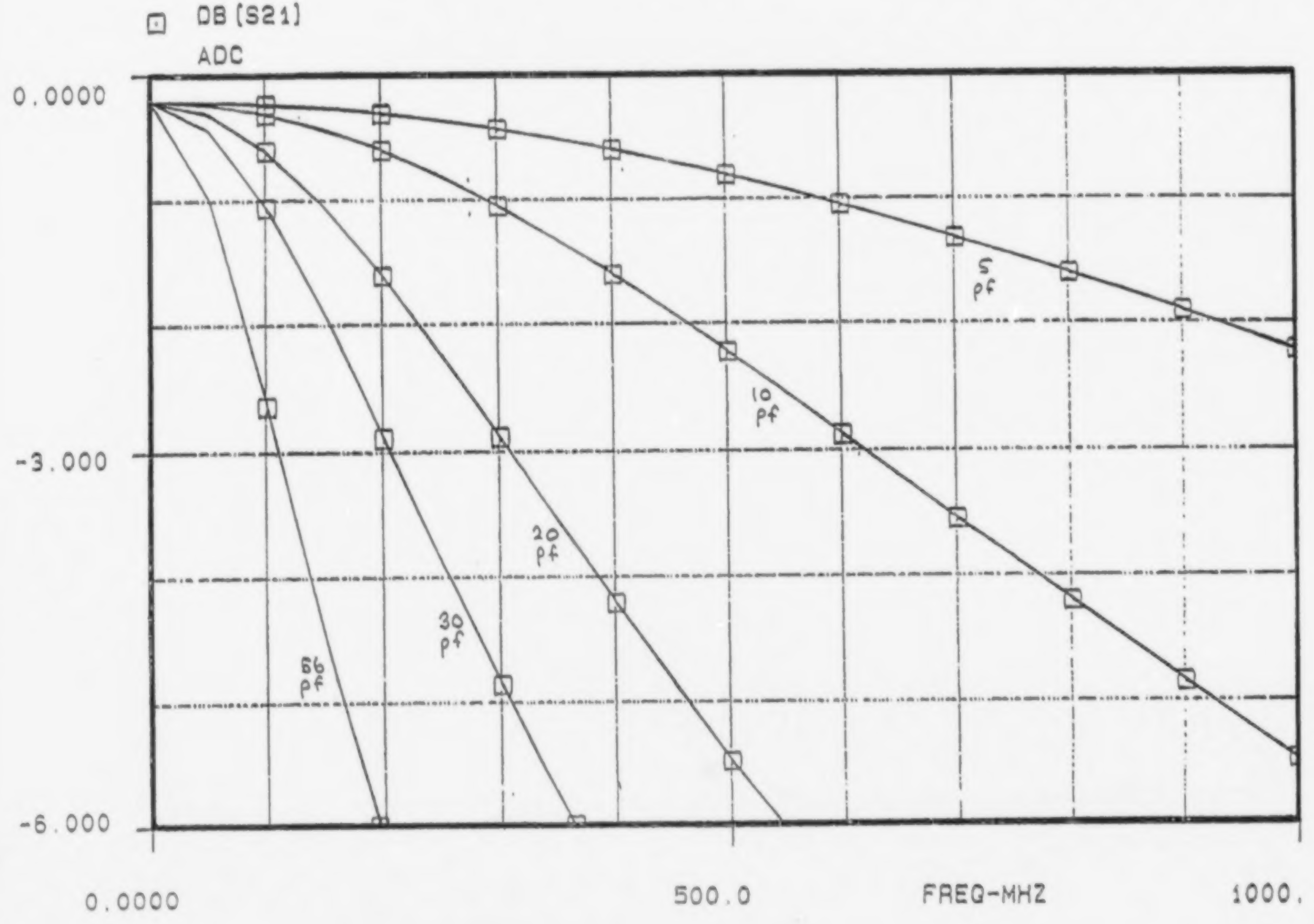


FIGURE 2.2.10 FLASH A/D INPUT FREQ. RESPONSE VS. INPUT CAPACITANCE

Hence an 8 bit resolution is reduced at the 3 dB point to about 7 1/2 equivalent bits. Figure 2.2.10 illustrates the 3 dB bandwidth of a flash converter based strictly upon its input capacitance. Table 2.2.2 summarizes the effect of the input capacitance.

C_{IN}(pf)	3 dB BW (MHz)
56	115
30	210
20	310
10	620
5	1200

Table 2.2.2 Variation of Bandwidth With Input Capacitance For A Flash Converter.

We can see that a 56 pf A/D has a 3 dB point at about 115 MHz.

Since more bits generally means more capacitance, flash converters are not well suited to very high input frequencies using present day technology. One common method to overcome this problem is to use a low source impedance buffer amplifier as shown in Figure 2.2.9(b). Figure 2.2.11 shows the 3 dB bandwidth of the 1KOhm//56pf flash A/D which would be achieved using a low impedance buffer amplifier. Table 2.2.3 summarizes the results.

Source Impedance Zo Ohms	3 dB BW MHz
50	55
20	135
10	280

Table 2.2.3 Variation of Bandwidth With Source Impedance For A Flash Converter.

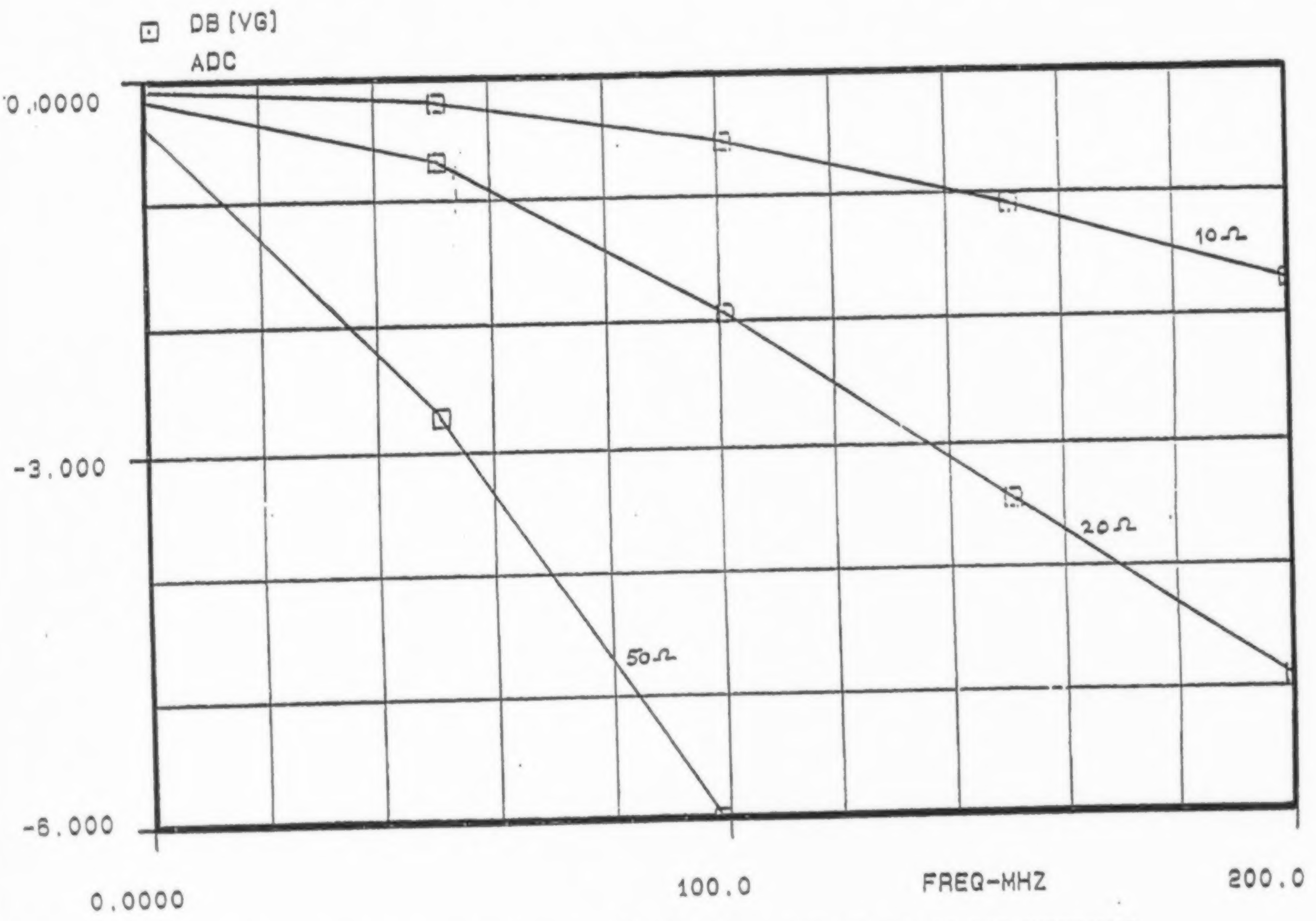


FIGURE 2.2.11 FLASH A/D INPUT FREQ. RESPONSE VS. BUFFER SOURCE IMPEDANCE

The low impedance buffer amplifier would appear to greatly enhance the flash converter performance. The problem is that at the moment DC coupled amplifiers with low source impedances are not available with bandwidths of greater than 140 MHz. The analog demux and S/H approach greatly reduces the input impedance problem. The input RF signal must now only see N parallel switches (in the off state) all in shunt with a 50 Ohm load.

In a typical parallel system, 12 flash converters each with input impedances of 1KOhm//27 pf can be used in parallel, while the input RF signal sees an input impedance at the demux of about 50Ohm//3pf. A simulated demux input impedance for a 1P12T is shown in Figure 2.2.12.

This front end has a 3 dB bandwidth of over 1 GHz. Since the input impedance of the parallel A/D is not a problem at high frequencies it then remains to build a S/H amplifier which can sample the demultiplexed analyzer pulse and hold the output voltage stable while the flash A/D samples the signal. For a typical flash A/D running at 100 MSPS with a 5 nsec set up and hold time the S/H amplifier must settle in under 5 nsec. This requires a slew rate of at least 1 Volt/nsec and a bandwidth of 50 MHz or greater. This is readily achievable with modern high slew rate operational-amps. An interesting feature of the parallel sampling system is that regardless of the input frequency this S/H amplifier always sees input pulses t_a psec wide (200 psec is typical). The input pulses are pulse amplitude modulated (PAM) signals, the modulation of the PAM pulses is essentially decoded by the S/H amp, the frequency of which varies between DC and $f_s/2N$ depending upon the input signal frequency. As long as the sampling system is designed such that $f_s/2N$ is sufficiently below the input bandwidth of the A/D for the number of bits being sampled then there is no effect upon the bandwidth and amplitude accuracy of the system from the flash A/D's.

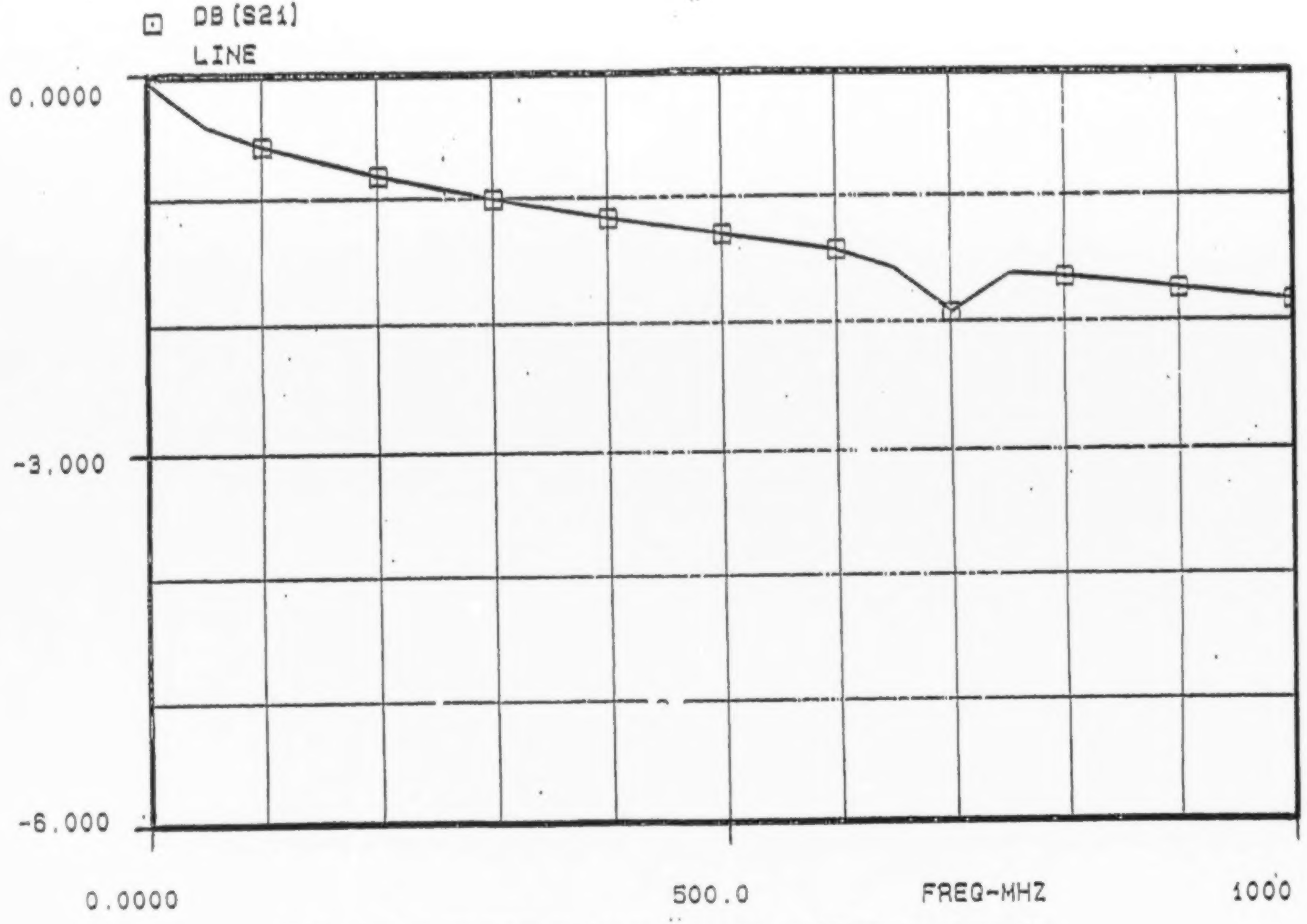


FIGURE 2.2.12 TELEMUS PARALLEL A/D INPUT FREQUENCY RESPONSE

The amplitude versus frequency response of the sampling system is limited by two factors. The first is the input impedance of the analog demux which was discussed earlier. The second factor is the effect of the sampling aperture width, t_a, upon the frequency response (see Appendix C). The TELEMUS parallel A/D utilizes a sampling aperture 200 psec wide which implies a 3 dB sampling bandwidth of 2.2 GHz. The simulated results of Figure 2.2.12 however indicate that the input parasitic impedances presently limit this 3 dB bandwidth to about 1 GHz.

Two examples of the aperture width requirements placed on a parallel system are as follows:

Example 1:

System Sampling Rate,	f_s	1000 Msps
Number of Parallel Channels	N	10
Resolution	n	8 bits
Channel Sample Rate	f_s/N	100 Msps
Demux Aperture Width	ta	200 psec
7.5 bit Response	$.44/t_a$	2.2 GHz
Effective Number of Bits at fin=500 MHz (fs/2)	n_{eff}	7.98
Highest Freq. Seen by flash A/D	$f_s/2N$	50 MHz
Req'd A/D Aperture Width	$t_{A/D}$	1.0 nsec
Max Settling Time for S/H Amp	$t_{S/H}$	9.0 nsec

Example 2:

System Sampling Rate	f_s	2100 Msps
Number of Parallel Channels	N	14
Resolution	n	4 bits
Channel Sample Rate	f/N	150 Msps
14 Channel Sample Period	N/f_s	6.67 nsec
Demux Aperture Width	t_a	200 psec

3 dB Input Frequency		2.2 GHz
for 4 bit response	f_{max}	1 GHz
Effective Number of Bits at fin = 1 GHz ($f_{s/2}$)	n_{eff}	4
Highest Freq. Seen by A/D		75 MHz
Req'd A/D Aperture Width	$t_{A/D}$	2.7 nsec
Max Settling Time for S/H Amp	$t_{S/H}$	4.0 nsec

A number of points can be made from these two examples. The first point is that aperture width requirements for the front end are increased proportionally versus 2^n or versus f. Hence doubling the bandwidth halves $t_{a(max.)}$, but doubling the number of bits, n, from 4 to 8 approximately quarters the value of $t_{a(max.)}$. We can also see the 3 way relationship between f_s/N, $t_{A/D}$ and $t_{S/H}$, that is:

$$N/f_s = t_{A/D} + t_{S/H.} \qquad \text{eq. (6)}$$

Obviously we can slow down the individual channel sample rate by increasing N for a given desired value of f_s. The physical limitations are imposed by the power, cost and physical space required for N parallel circuits. The bandwidth restrictions are placed by the parasitic impedances of a 1PNT demux attempting to sample signals at $f_s/2$ to n bits accuracy. Hence, for reasons of power, cost and size we will attempt to minimize N to the least required number to attain our goal of a sampling rate of f_s. This almost always means utilizing the fastest commercially available, n bit, flash converter. Normally if the maximum usable sample rate of the flash converter is $f_{A/D}$ and the required system sample rate is f_s, then we need $f_s/f_{A/D} = N$, where N is an integer. A problem with this solution may arise if the selected flash converter aperture width, $t_{A/D}$, is a large proportion of the channel sample time, N/fs. We can see from equation (6), that this puts an unrealistic demand on the S/H amplifier. The solution is to increase N or select a flash converter with a smaller aperture width, t_a.

We can see from the design example 1 that the selected 8 bit, 100 MSPS flash converter must have an aperture width of 1 nsec maximum and the S/H amp must settle to 8 bits accuracy in 9 nsec. In the second example the 4 bit, 150 MSPS flash converter only needs to have a 2.7 nsec aperture width but the S/H amplifier must settle to 4 bits accuracy in 4.0 nsec. If the settling time requirement is too fast for the S/H amplifier one trade off might be to use a more expensive 8 bit flash converter with a 1 nsec aperture time, but only use the top 4 bits. This would then allow the S/H amplifier 5.7 nsec to settle to 4 bits accuracy. As we can see from these examples, when attempting to minimize the number of channels in a parallel sampling system, one of the most critical areas of the design is the S/H amplifier settling time.

TELEMUS utilizes proprietary S/H amplifiers in our parallel A/D designs. The TELEMUS S/H features aperture times of 200 picoseconds, slew rates of 5 volts/nanoseconds and settling times to 4 bits accuracy in under 2 nanoseconds.

2.2.4.3 A/D Converter Trade Off Considerations

After analyzing all the different A/D architectures and some specific parameters, we can conclude that the major trade-offs when selecting an A/D is quantization, conversion speed, and cost. Since A/D selection is based on a particular application, we cannot go any further at this poi in trying to discuss every possible trade-off. However, Table 2.2.4 summarizes qualitatively the different architectures in terms of the most critical parameters. Table 2.2.5 lists a current survey of state-of-the-art A/D's.

When selecting an A/D there are many parameters to consider. Depending on a particular application, it is possible to find the appropriate device. But sometimes meeting the right requirements is not enough to achieve the optimum performance. Some dynamic performance testing of A/D converters is required. These

PARAMETER	CONVERTER		ARCHITECTURES		
			FEEDBACK		FEEDFORWARD
	FLASH	SUCCESSIVE APPROXIMATION	SERIES-SUBRANGING	SERIES-PARALLEL	SERIES OR PARALLEL
QUANTIZATION BITS	8 TO 10	8 TO 16	8 TO 12	10 TO 12	4 TO 12
DIGITIZATION SPEED	10 TO 300 MHZ	<400 KHZ	1 TO 10 MHZ	1 TO 20 MHZ	UP TO 10 MHZ
TECHNOLOGY	ECL	CMOS OR TTL	ECL + TTL	ECL + TTL	ECL + TTL
COMPLEXITY OF ARCHITECTURE	LOW	LOW	MEDIUM	HIGH dep. on # of FLASHES	HIGH dep. on # of BITS
COMPLEXITY OF USING DEVICE	COMPLEX INTERFACING	SIMPLE INTERFACING	SIMPLE	SIMPLE	AVERAGE TO HIGH COMPLEXITY
COST	RELATIVELY EXPENSIVE	AVERAGE COST	LOW COST	AVERAGE COST	RELATIVELY EXPENSIVE
ERROR SOURCES	VERY LOW	AVERAGE	LOW	AVERAGE	HIGH
INPUT IMPEDANCE	LOW	HIGH	MEDIUM	MEDIUM	LOW TO HIGH
INPUT BANDWIDTH	WIDE	SMALL	MEDIUM	MEDIUM	MEDIUM
APERTURE TIME	VERY SMALL <200 psec.	VERY LARGE few usec	SMALL few nsec	SMALL few nsec	SMALL TO VERY SMALL
APERTURE JITTER	VERY SMALL <10 psec.	LARGE few usec.	SMALL few nsec.	SMALL few nsec.	SMALL TO VERY SMALL
LINEARITY	GOOD	POOR for large # bits	GOOD	GOOD	AVERAGE

TABLE 2.2.4 A/D CONVERTER ARCHITECTURES AND ASSOCIATED PARAMETERS

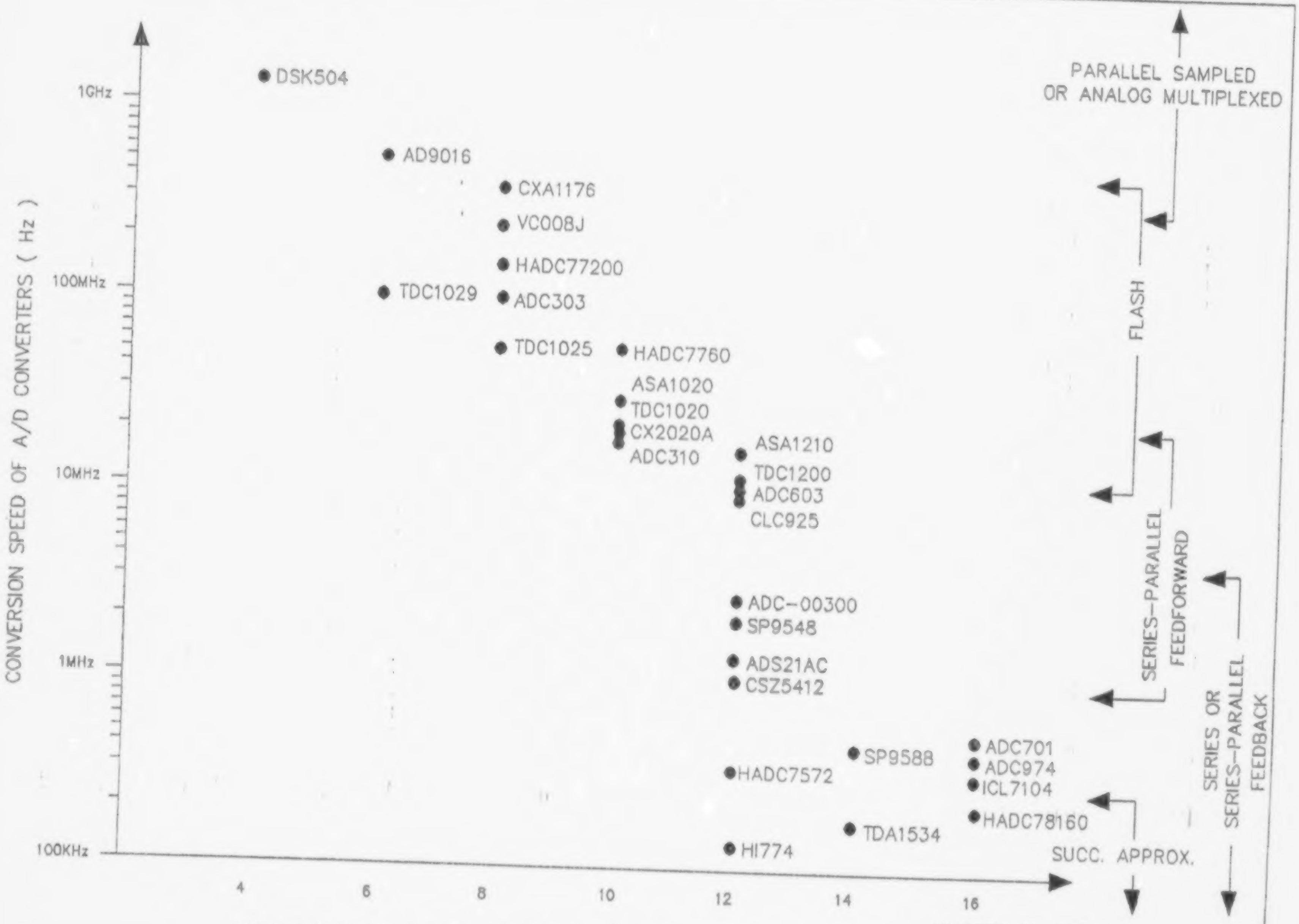


TABLE 2.2.5 SURVEY OF THE STATE OF THE ART A/D CONVERTERS

performance tests are listed in Table 2.2.6 and a description on each test is found in Appendix F.

2.2.5 Driver Circuitry

A driver circuit is normally used in front of an A/D for three main reasons:

a) Improve the sampling response
b) Improve the signal bandwidth using impedance transforming, and
c) Level shift and/or amplify the input signal so that the full dynamic range of the A/D is used.

As we are going to see in the sections that follow, reason a) depends more on the sampling aperture width of the driver and aperture jitter. Reason b) is a function of the input impedance of the A/D, therefore a driver should be able to follow very fast input signals while supplying this signal to very low impedances at the output. Reason c) deals with signal amplitude levels and therefore dynamic range.

From a survey of A/D converters we concluded that the requirements for a driver in an A/D is usually related to its architecture, and this is illustrated in Table 2.2.7

From Table 2.2.7 only the flash type of converter might require all three types of drivers (depending on the application). Most of the other converter architectures have the drivers built into the same chip package, but there are some exceptions where the sample/hold amplifier must be supplied externally.

With this in mind we can now proceed to analyze some of the more critical parameters that a driver should be able to meet without degrading the performance of the analog to digital converter.

TESTS

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes—shows up as spikes	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Missing Codes	Yes—shows up as bins with 0 counts	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Integral Nonlinearity	Yes (could be measured directly with a highly linear ramp waveform)	Yes—shows up as harmonics of fundamental aliased into baseband	Yes—part of rms error	Yes
Aperture Uncertainty	No—averaged out. Can be measured with "locked" histogram.	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Noise	No—averaged out. Can be measured with "locked" histogram.	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Bandwidth Errors	No	No	No	Yes—used to measure analog bandwidth.
Gain Errors	Yes—shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes—shows up in offset of distribution average.	No	No	No

TABLE 2.2.6 PERFORMANCE TESTS REQUIRED WHEN SELECTING A/D CONVERTERS

ARCHITECTURE	DRIVER TYPE		
	S/H OR T/H	TRANSIMPEDANCE AMPLIFIER	REFERENCE CIRCUITRY
FLASH	NOT REQUIRED (MAY BE REQUIRED ONLY FOR UNDERSAMPLING OR WIDE BANDWIDTHS)	REQUIRED (TO SHIFT INPUT VOLTAGE AND BW IMPROVEMENT)	REQUIRED (TO SUPPLY RESISTOR CHAIN)
SUCCESSIVE APPROXIMATION	REQUIRED	NOT REQUIRED (INPUT AMPLIFIER IS WITHIN THE CHIP)	NOT REQUIRED (INCLUDED IN THE PACKAGE)
SERIES-FEEDBACK (SUB-RANGING)	REQUIRED (USUALLY IN THE CHIP)	NOT REQUIRED (IN THE SAME CHIP)	NOT REQUIRED (INCLUDED IN THE PACKAGE)
SERIES-PARALLEL FEEDBACK	REQUIRED (USUALLY EXTERNAL)	NOT REQUIRED (IN THE SAME CHIP)	NOT REQUIRED (INCLUDED IN THE PACKAGE)
SERIES FEEDFORWARD	REQUIRED (USUALLY IN THE SAME CHIP)	NOT REQUIRED (IN THE SAME CHIP)	NOT REQUIRED (INCLUDED IN THE PACKAGE)
SERIES-PARALLEL FEEDFORWARD	REQUIRED (USUALLY IN THE SAME CHIP)	NOT REQUIRED (IN THE SAME CHIP)	NOT REQUIRED (INCLUDED IN THE PACKAGE)

NOTE: Parallel sampled A/Ds and analog multiplexed A/Ds are usually constructed with any of the architecures shown above.

TABLE 2.2.7 DRIVER REQUIREMENT ON DIFF. ARCHITECTURE OF ADC

2.2.5.1 Sample/Hold Or Track/Hold

Sample/hold and track/hold amplifiers are used when the voltage level of a signal must be held or stored for a short period of time to allow the A/D conversion to take place. This is a must for a feedback or feedforward architecture because the aperture width is usually the same length as the sampling time, therefore the input signal will change during the conversion causing excessive amplitude variation. In the case of a flash A/D, the S/H or T/H amplifier might be used to improve the sampling response by choosing a S/H or T/H with an aperture width T_a smaller than the A/D aperture width. Figure 2.2.13 relates input signal frequency, percentage of quantizing error and aperture width. The end result of having a small aperture width is to extend the input signal bandwidth for the same percentage error as Figure 2.2.13 illustrates.

The aperture width of a T/H should be chosen to given ±1/2 LSB of the A/D maximum error at a given bandwidth.

The main components of a S/H or T/H amplifier are shown in Figure 2.2.14. The difference between an S/H and T/H amplifier is that a sample/hold can only sample the input signal briefly, whereas a track/hold can track the input continuously. In an S/H the gate is AC coupled to the switch, and the switch can remain closed for only a brief time. In a T/H the gate is DC coupled to the switch, and the switch remains closed as long as the gate signal stays in the track mode.

The relationship between the output, input, and gate signals of an S/H or T/H amplifier are complex. In these devices there are delays between the gate signal changes and the opening or closing of the switch. Time is required for the output to settle, the output can have offsets and input signals can feed through to the output even when the switch is open. These effects are illustrated in Figure 2.2.15.

$$n_{eff.} = n - (\%\ \mathrm{err.})n$$

$$\%\mathrm{err.} = 100 \left[1 - \frac{\sin(\pi f_{in} T_a)}{\pi f_{in} T_a} \right]$$

where: $n_{eff.}$ = effective number of bits

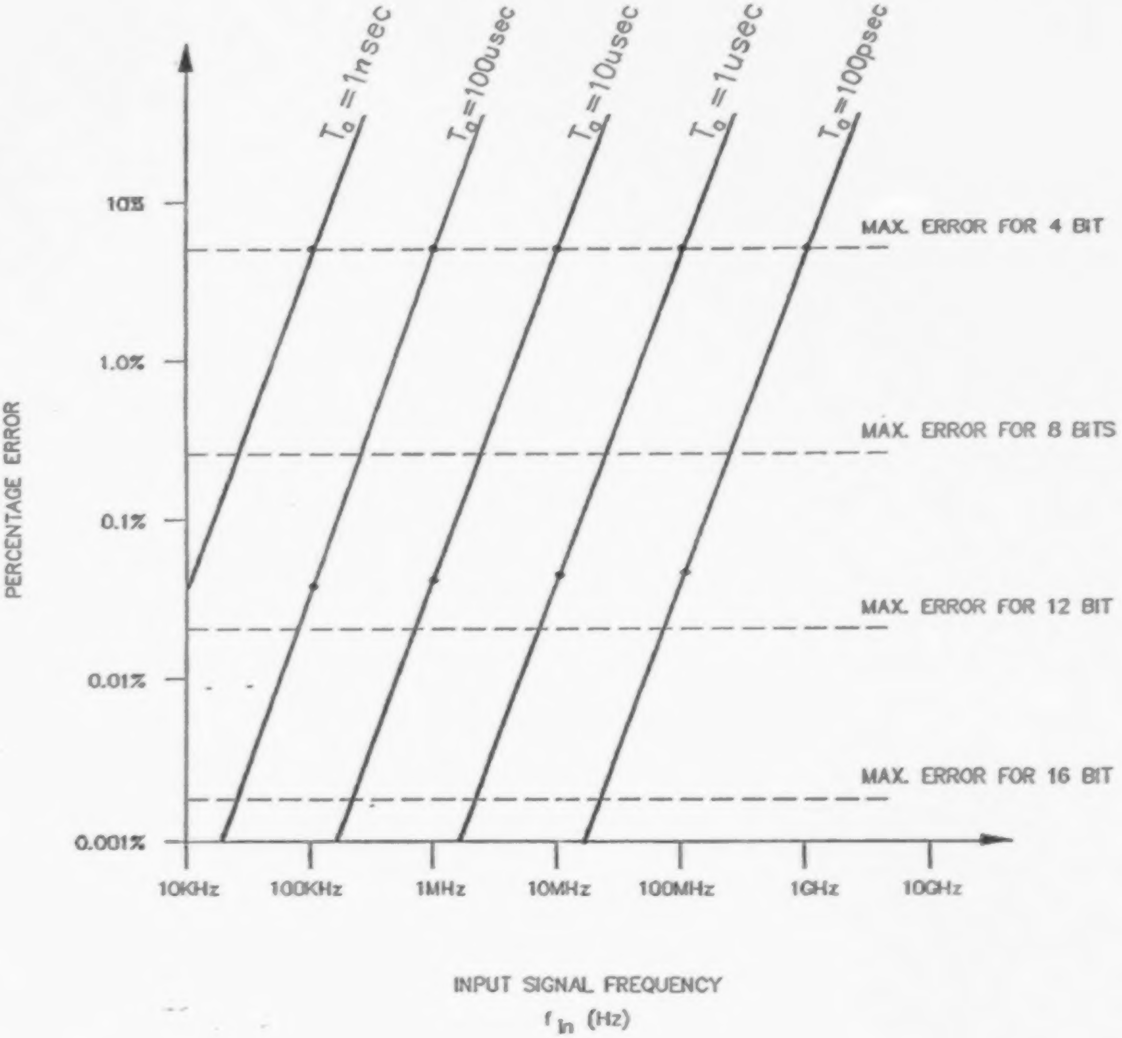
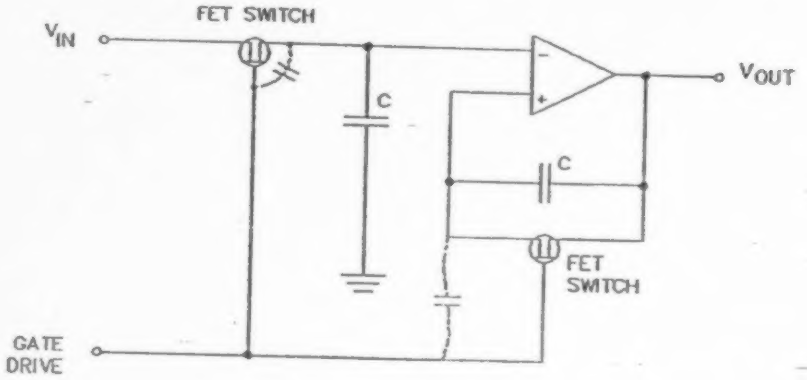
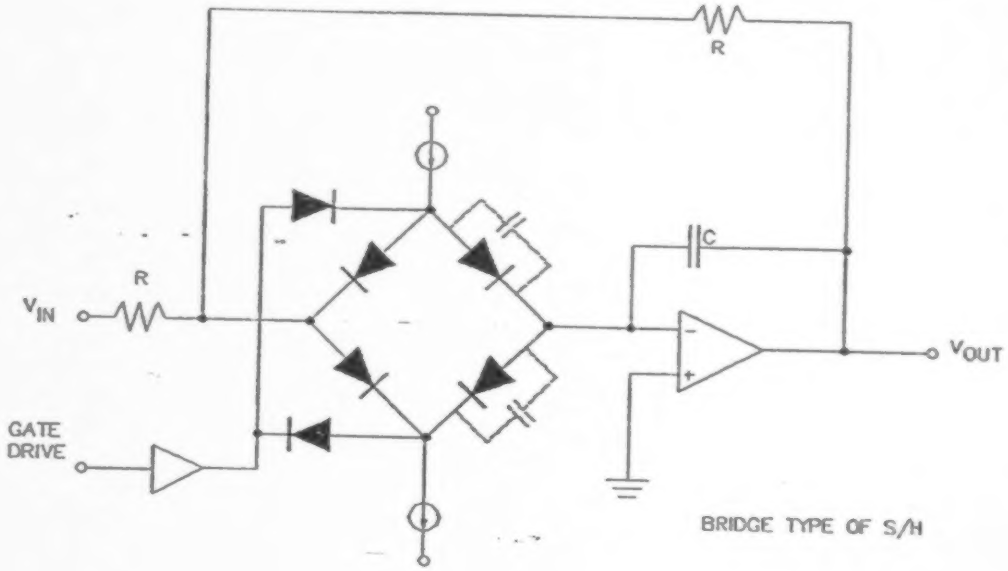


FIGURE 2.2.13 APERTURE WIDTH AND EFFECT ON NUMBER OF BITS AT DIFFERENT INPUT SIGNAL FREQUENCIES



FET TYPE OF S/H



BRIDGE TYPE OF S/H

FIGURE 2.2.14 S/H OR T/H AMPLIFIERS

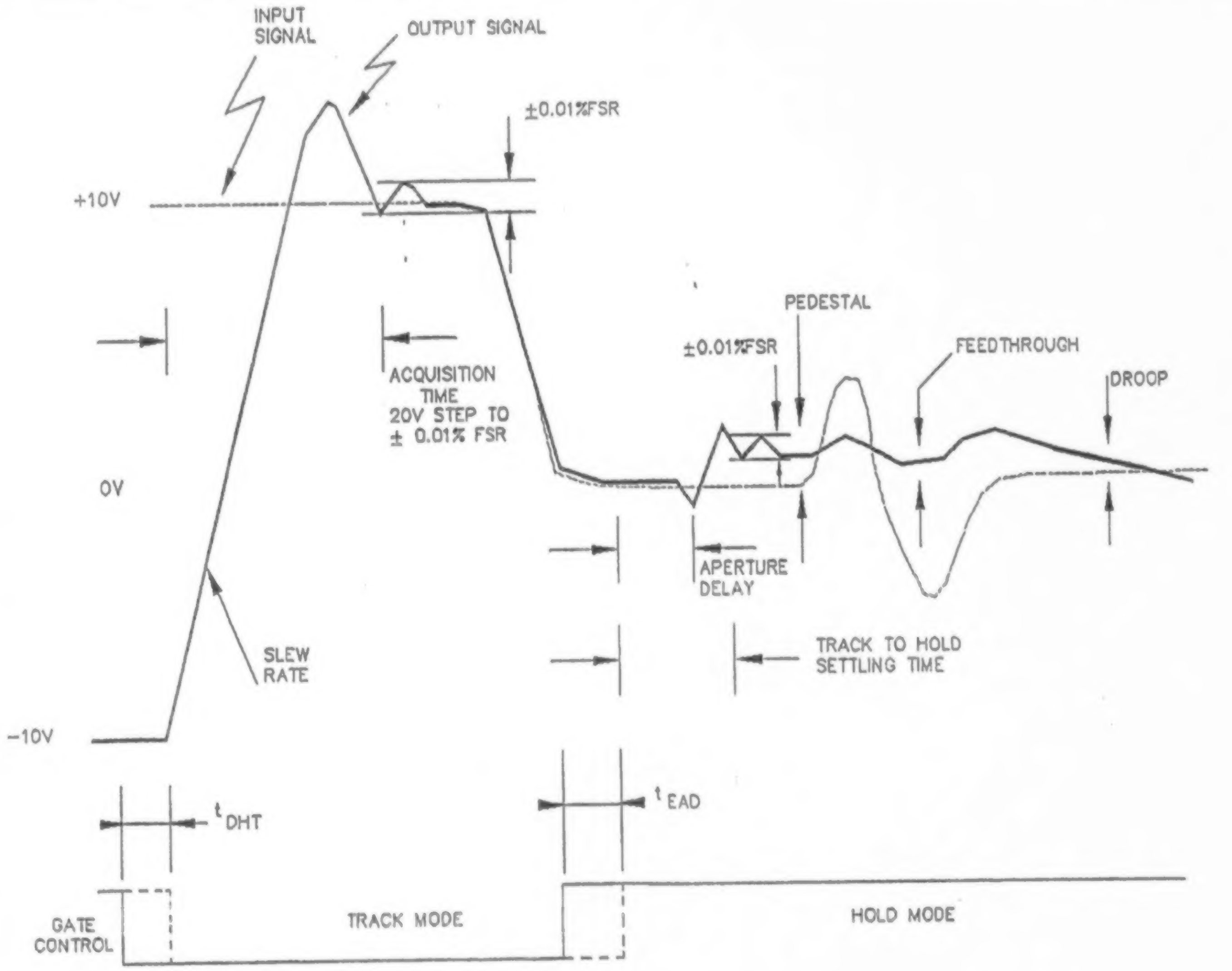


FIGURE 2.2.15 RELATIONSHIP OF OUTPUT, INPUT AND GATE SIGNALS

2.2.5.1.1 Matching A T/H Or S/H To An A/D Converter

High performance broadband S/H or T/H come in two versions: Junction FET and diode bridge type (see Figure 2.2.14). Diode bridge devices more readily accommodate applications that call for short RC time constants emphasizing speed rather than accuracy. For more demanding applications, FET-type sample/hold amplifiers yield superior performance. Accuracy results from the use of two FET switches, both of which help cancel the charge-injection error caused by the gate's drive waveform, permitting a low hold capacitor value. Additional FET type sample/hold amplifier advantages include higher input impedance than diode bridge types and the elimination of offset bias and feedback resistors. And because FET sample/holds exhibit much lower leakage than diode bridge units as well as a balanced configuration, the FET type's output buffer amplifier contributes virtually no leakage current. Table 2.2.8 summarizes the characteristics of diode-bridge and FET sample/hold amplifies.

When a S/H or T/H amplifier is used at the input of an A/D, the performance of the system will depend on the combined specifications of both units, as well as on their compatibility.

2.2.5.1.2 Sampling Rate Limitations

The sampling rate is the rate at which an entire sample and hold cycle is completed.

$$\text{Sampling rate} = \frac{1}{T_{TRACK}\ (\text{or sample}) + T_{HOLD}} \qquad \text{eq. (7)}$$

The T/H worse-case clock rate and duty cycle are obtained by independently determining the minimum required "track" and "hold" times. Since sufficient time must be provided for all events to take place within their respective periods, the timing equations can be determined from the waveforms of Figure 2.2.15. These are:

DIODE BRIDGE TYPE	FET TYPE
Lower charge injection error	Greater DC accuracy; has no offset and doesn't need feedback resistors.
Less generation of spikes; lower drive voltages are needed for bridge switching.	Faster in higher voltage applications; offers large slewing current.
Shorter aperture delay; Diodes switch faster than FET's.	Smaller droop; exhibits less inherent leakage.

TABLE 2.2.8 CHARACTERISTICS OF DIODE BRIDGE AND FET SAMPLE/HOLD AMPLIFIER

$$T_{TRACK} = t_{ACQ} + t_{DHT} - t_{EAD} - t_{DA} \qquad \text{eq. (8)}$$

$$T_{HOLD} = t_{S} + t_{A/D} - t_{DHT} + t_{EAD} + t_{DA} \qquad \text{eq. (9)}$$

where $t_{A/D}$ is the aperture time of the A/D and t_{ACQ} is the acquisition time of the T/H while driving the capacitive input of the A/D (not the value which is specified into a purely resistive load). The minimum T/H cycle time is simply the sum of the above equations:

$$t_{cycle}(\text{min.}) = t_{ACQ} + t_{s} + t_{A/D} \text{ [Ideal case]} \qquad \text{eq. (10)}$$

Note that the three delay terms are "pipelined" out of the system. Operation of the T/H at this minimum cycle time represents a problem caused by manufacturing variations of the T/H and A/D. Again, since sufficient time must be allowed for all events, the worst-case T_{TRACK} and T_{HOLD} times should be used in the system set-up if the system must work without timing adjustments. Now, however the sum of equations (8) and (9) no longer equals equation (10). A more accurate expression for minimum cycle time is:

$$t_{CYCLE}\ (\text{min}) = [T_{ACQ} + t_{s} + t_{A/D}] + [\ dt_{OHT} + dt_{EAD} + dt_{DA}] \qquad \text{eq. (11)}$$

A T/H has a maximum cycle time which is a function of the "Droop" rate. The droop rate is a specification of nonlinearity caused during the hold mode of operation. The output error will exceed the specified accuracy if the hold time is greater than the maximum error divided by the droop rate. Droop may eventually cause the output voltage to exceed the limits of the specified output voltage range. The time to acquire a new signal may then exceed the specified acquisition time because of saturation effects. Figure 2.2.16 relates percentage error for an n-bit digitization and droop rates for different sampling rates. As a target, the T/H or S/H chosen should have droop less than 1/2 LSB from the time the amplifier enters the hold mode to when the A/D completes conversion.

INPUT VOLTAGE = ±1.0 VOLTS

∴ INPUT FSR = 2.0 VOLTS

$$\%err = 100X \frac{D_{RATE}}{FSR} \times \frac{1}{f_{SAMPL}}$$

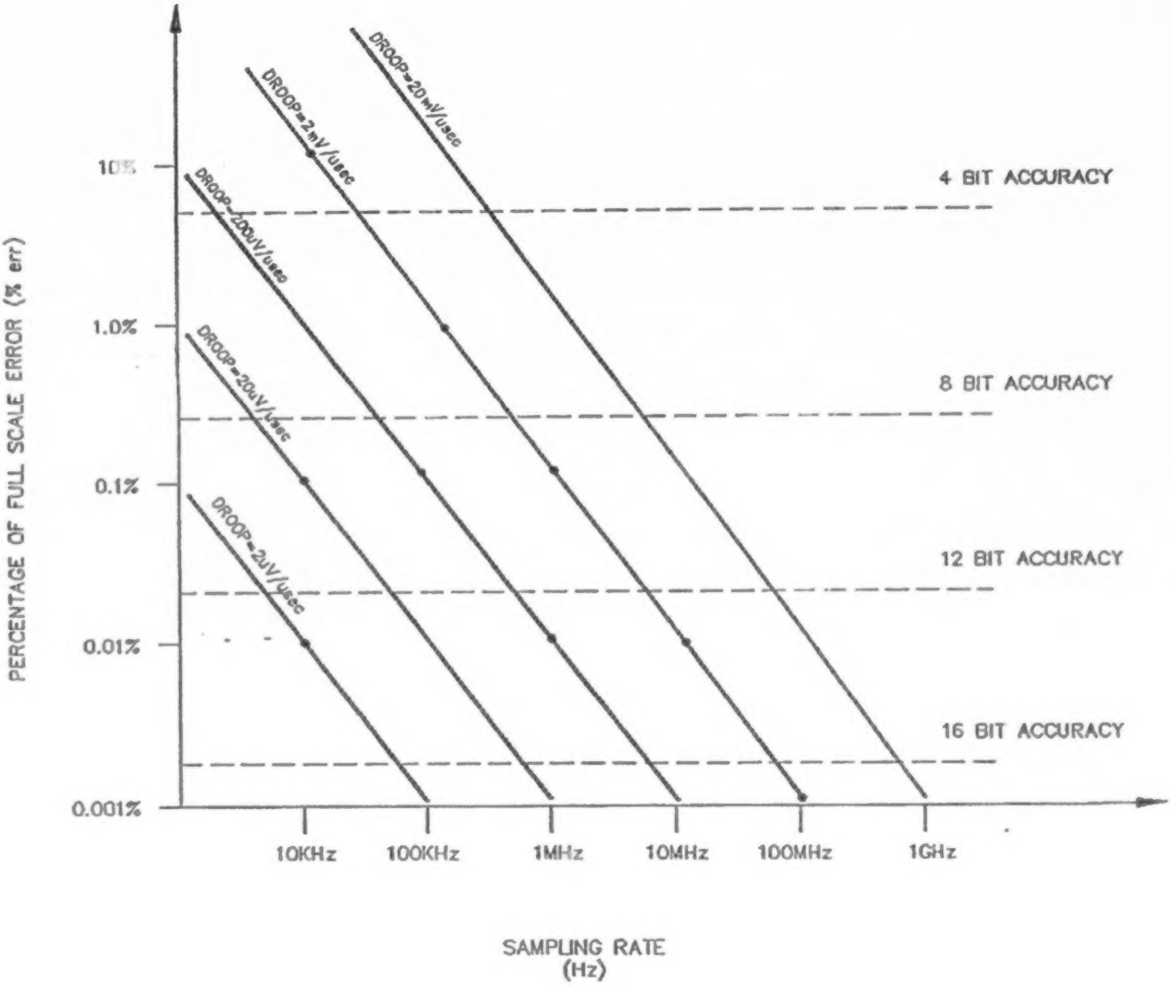


FIGURE 2.2.16 EFFECT OF DROOP RATE ON OUTPUT ERROR AS A FUNCTION OF THE SAMPLING RATE

2.2.5.1.3 Aperture Time Uncertainty

The uncertainty in the moment of time at which the signal is acquired and held (the aperture time jitter) causes an error whose magnitude depends on the rate at which the input is changing. This specification is a non-linearity caused during the transition from track to hold mode. See Appendix E.

The error caused by aperture time uncertainty may be obtained from Figure 2.2.17 if the input is sinusoidal and the output is not slew rate limited. This plot therefore relates the corresponding aperture uncertainty, percent full scale error, and input signal frequency.

The maximum percentage error allowed by the T/H should be less than ± 1/2 LSB of the A/D converter for optimum performance.

2.2.5.1.4 Feedthrough Rejection

Feedthrough rejection, another hold-mode specification, has the potential for degrading accuracy by causing the held voltage level to change as the analog input to the T/H or S/H continues to change. Feedthrough rejection can degrade if power supply bypassing is not properly done. As a rule of thumb, feedthrough rejection should represent less than ± 1/4 LSB of the A/D at the maximum input signal frequency. For instance, suppose the converter has 8 bit resolution (1 LSB = 0.4%) and an 18 MHz clock rate. Then $f_{SIGN(max)}$ is 9 MHz, and at this frequency the sample/hold should have a maximum feedthrough rejection of 0.1% (60 dB). Figure 2.2.18 illustrates a typical performance evaluation curve for the feedthrough rejection of sample/hold amplifiers. Note as the allowed error curve moves to the right, for the same feedthrough rejection ratio, we get a drop in the effective number of bits.

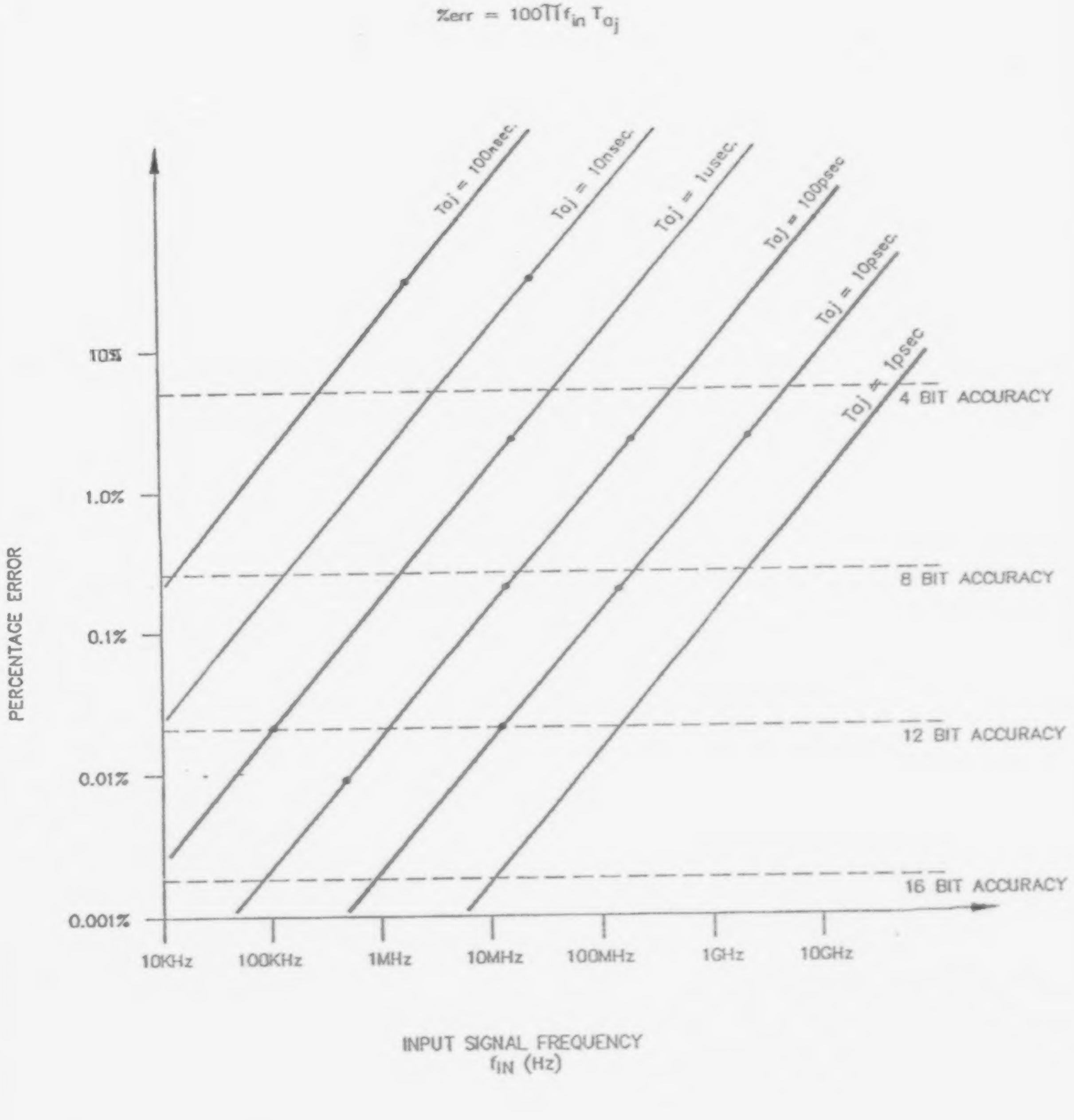


FIGURE 2.2.17 ERROR CAUSED BY APERTURE TIME UNCERTAINTY ON INPUT SIGNAL

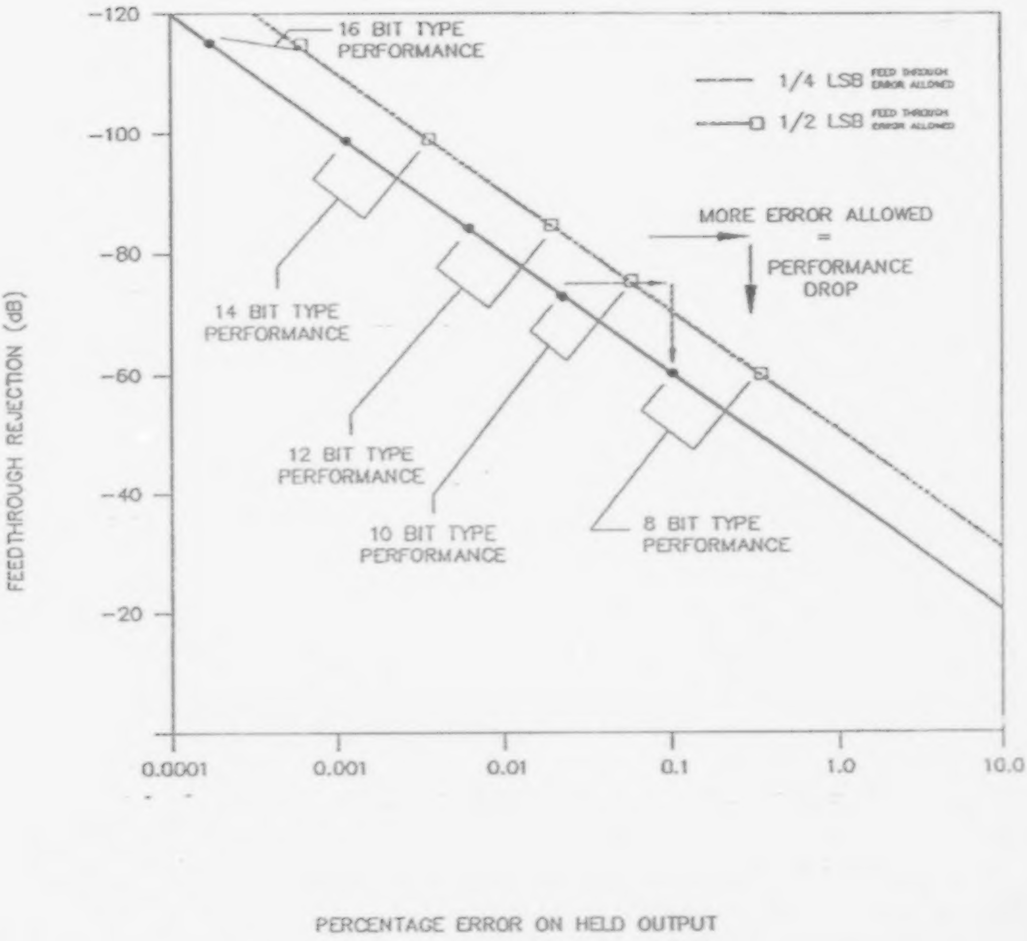


FIGURE 2.2.18 ERROR CAUSED BY FEEDTHROUGH SIGNAL ON HELD VOLTAGE

2.2.5.1.5 Linearity

Linearity and dynamic accuracy form another set of specifications usually evaluated in conjunction with the timing specifications. DC linearity is of some interest since a device cannot be relied upon to deliver better dynamic accuracy than it can at DC. More important is the harmonic distortion specification, which is an indication of the linearity of the amplifiers within the T/H amplifier at high analog frequencies. Both of these linearity specifications describe operation in the track mode.

Harmonic distortion is measured with the device in the track mode, it gives only an estimate of true performance in a sampled data system. The specification includes none of the switching dynamics which occur in the dynamic sample-mode where the T/H toggles repeatedly between the track and hold modes. Actual dynamic performance, being a function of these switching dynamics, will depend on the clock signals supplied to both the T/H and A/D. When operating with conservatively chosen clock signals, the T/H performance can be expected to closely approach these distortion levels given by the manufacturer. However, as the cycle time approaches the minimum as determined above, the distortion levels will worsen. Manufacturers prefer not to specify dynamic sample-mode harmonic distortion because of the difficulty of the measurement and its dependence upon more application-specific variables compared to the simple track-mode harmonic distortion test.

Part of the difficulty encountered in measuring dynamic sample-mode harmonic distortion is in finding a high speed quantizer having an accuracy that will not limit the performance of the T/H. This problem is especially acute since T/H's are used to improve quantizer accuracy. Not only does this quantizer require resolution and linearity exceeding that of the T/H under test, aperture time should also be insignificant so that it does not limit cycle time. In addition, the load impedance it presents to the T/H should be adequate to allow the designer flexibility in simulating various loading on the T/H output. A quantizer system meeting these requirements can be constructed using a latching comparator with integrator feedback as described in Reference [1]. Usually selection of a T/H is based upon available data sheet information and evaluation of the chosen device as part of the overall system. Trade-offs between the two approaches are obvious.

2.2.5.1.6 Output Loading

T/H output loading is one of the variables affecting harmonic distortion and DC nonlinearity. For the sake of maximum speed, most high-speed T/H designs utilize open-loop buffer amplifiers and, therefore, function best with as high a load impedance as possible. Because of this, it is best to avoid transmission lines and long traces between the T/H output and the A/D input.

Also related to loading is the fact that high-speed amplifiers do not yield their best settling times when operating into the highly capacitive input of flash A/D converters without some assistance. Typically, this assistance is simply a series damping resistor placed between the T/H and A/D. The value of this resistor is, of course, important in minimizing acquisition time. Too small a value will cause excessive ringing and too large a value will excessively overdamp the output.

Another type of assistance (Section 2.2.5.2) is by inserting a transimpedance amplifier between the T/H and the A/D.

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[1]. J. Halbert and M. Koen "A Waveform Digitizer for Dynamic Testing of High Speed Data Conversion Components" International Test Conference of the IEEE, paper 20.2 1983

2.2.5.1.7 Conclusion

A T/H or S/H amplifier is an essential device in a data acquisition system whether it is built into the A/D package or it is supplied as an external component.

From a survey it was found that most of the slow speed A/D's require an S/H to be supplied externally. The medium speed A/D's have a built-in T/H amplifier while the high speed A/D's (flash type) require a T/H to be supplied as an external component as well.

From previous discussion it was shown that parameters such as aperture time, uncertainty, feedthrough and acquisition becomes critical when high speed acquisitions with large bandwidths are performed. Therefore, in order to achieve optimum performance, the parameter selected for a T/H should not allow this error to exceed the one shown by the plots discussed in the analysis. (Table 2.2.9 summarizes these errors)

Also T/H amplifiers are poor drivers of high capacitive loads normally found in flash A/D's, therefore a post driver such as a transimpedance amplifier must be inserted between a T/H and an A/D.

Finally, cost of T/H or S/H amplifiers vary, depending on the sampling speed. The higher the sampling speed, the higher the cost of the device. Table 2.2.10 summarizes the current survey of T/H or S/H amplifiers available on the market.

2.2.5.2 Transimpedance Amplifier

From our previous discussion, we concluded that an input driver other than a T/H or S/H amplifier would be required in front of an A/D converter when high-speed data acquisition is performed. As we already mentioned in Section 2.2.5 (Table 2.2.7) driver requirements are usually architecture dependant.

SOURCE OF ERROR	MAXIMUM ERROR ALLOWED IN LSB
Droop Rate Error	± 1/2
Aperture Uncertainty	± 1/2
Linearity	± 1/2
Feedthrough Rejection	± 1/4
Acquisition time to settle	± 1/2
Aperture width - (Sampling Response Bandwidth)	± 1/2

TABLE 2.2.9 MAXIMUM ERRORS ALLOWED FOR OPTIMUM PERFORMANCE

T/H OR S/H DEVICE	ACQUISITION TIME (nsec.)	FEEDTROUGH (dB)	APERTURE JITTER (psec.)	DROOP RATE (μV/usec.)	LINEARITY % F.S.R.	BANDWIDTH (small signal)
MICRONETWORK MN379	35 5V. ± 0.1 %	60	1	500	± 0.1 %	100 MHz
MICRONETWORK MN376	160 10V. ± 0.01 %	78	40	± 0.5	± 0.01 %	16 MHz
MICRONETWORK MN375	700 2.5V. ± 0.005 %	78	100	± 0.5	± 0.005 %	5 MHz
COMLINEAR CLC940AL	16 2V ± 0.1 %	74	1	20	± 0.02 %	150 MHz
CRYSTAL CS3112	1000 6V ± 0.1 %	58	100	± 1	± 0.001 %	2.5 MHz
SIPEX SP5330	500 5V ± 0.01 %	60	100	10	± 0.005 %	2 MHz
SIPEX HS9720	200 5V ± 0.01 %	80	50	500	± 0.02 %	13 MHz
BURR-BROWN SHC-600	50 2.5V ± 0.02 %	58	5	± 180	± 0.01 %	70 MHz
BURR-BROWN SHC-702	600 10V ± 150 uV	100	10	± 2	± 0.0003 %	3.1 MHz
TELEMUS SH1200	0.200 2V + 0.1 %	70	0.5	N/A	+ 0.02 %	2.0 GHz

TABLE 2.2.10 SURVEY OF STATE OF THE ART T/H OR S/H AMPLIFIERS

In this analysis we shall concentrate on drivers needed in flash converters since these are used in high-speed data acquisition system. This requires careful attention of the parameter selection. From Table 2.2.7 we can see that other A/D converters have built-in input voltage drivers and in most cases the gain is programmable. Therefore, the performance of the A/D is already optimized for the particular speed and bandwidth of operation. Figure 2.2.19 summarizes the different architectures of digitization highlighting the drivers required at different speed of acquisition. The illustration basically reflects the requirements described by Table 2.2.7 . With this in mind then we proceed to describe the most crucial parameters for the input voltage driver needed by a flash A/D.

Information can easily be distorted when some amplifiers and buffers are employed. In many cases, these devices serve as low pass filters and introduce harmonic distortion.

Flash converters require drivers that exhibit two major attributes. First, sufficient bandwidth at the desired gain is imperative. Secondly, it is necessary for the amplifier to be able to drive very large (and sometimes variable) capacitive loads. A transimpedance amplifier meets both of these criteria nicely and is an excellent choice to drive flash A/D converters. (See Appendix G for typical theoretical parameters of transimpedance amplifier).

2.2.5.2.1 System Bandwidth Requirement

Some of the greatest challenges in high speed A/D conversion involve the drive circuitry. Ideally, the analog signal path would have an overall bandwidth equal to the Nyquist frequency to avoid aliasing problems. Due to a prior lack of commercially-available DC coupled amplifiers with sufficient high frequency performance, in many applications the amplifier has acted, by default, as the low pass (anti-aliasing) filter. To limit bandwidth, however, by

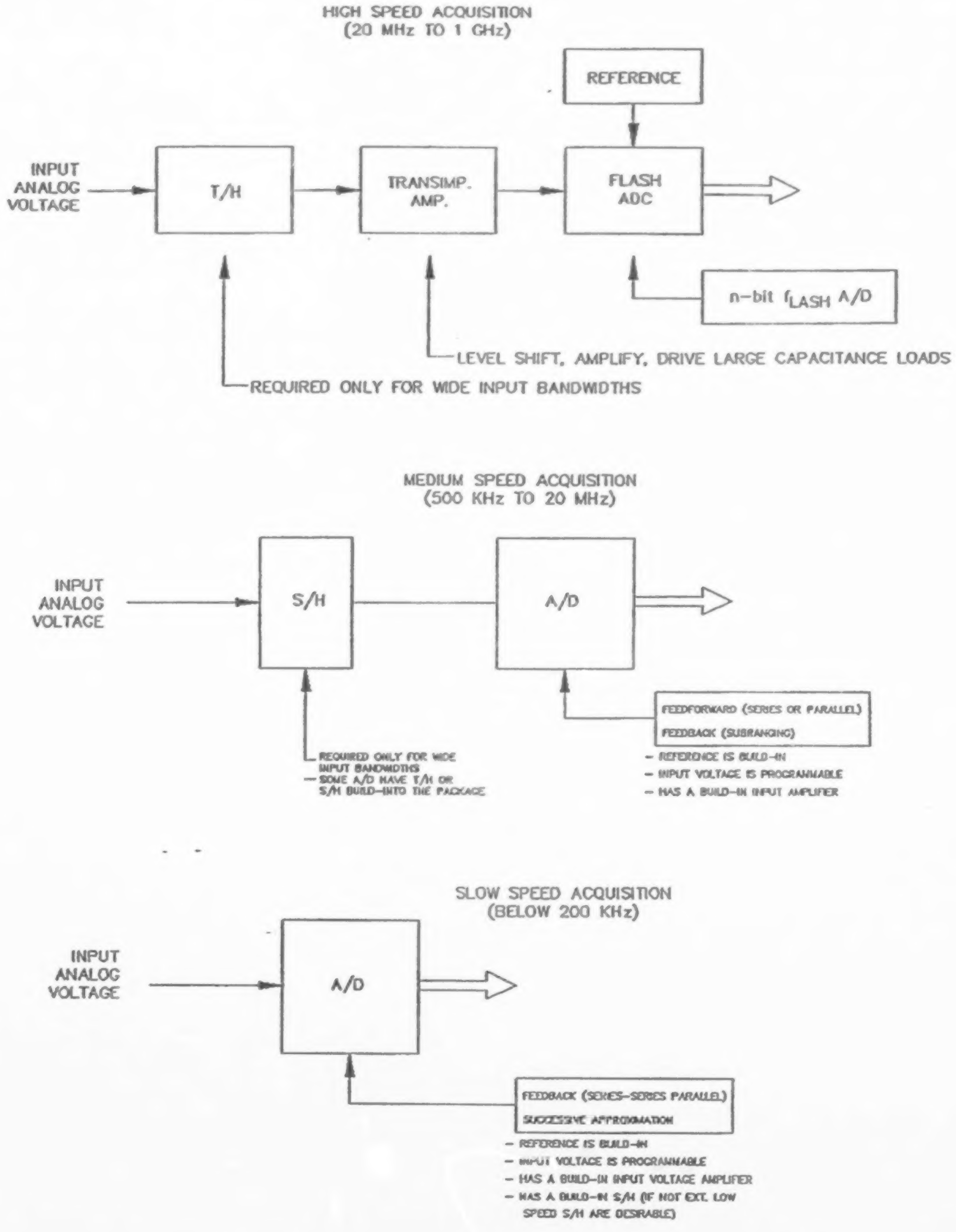

HIGH SPEED ACQUISITION
(20 MHz TO 1 GHz)
REFERENCE
INPUT ANALOG VOLTAGE
T/H
TRANSIMP. AMP.
FLASH ADC
n-bit fLASH A/D
LEVEL SHIFT, AMPLIFY, DRIVE LARGE CAPACITANCE LOADS
REQUIRED ONLY FOR WIDE INPUT BANDWIDTHS
MEDIUM SPEED ACQUISITION
(500 KHz TO 20 MHz)
INPUT ANALOG VOLTAGE
S/H
A/D
FEEDFORWARD (SERIES OR PARALLEL)
FEEDBACK (SUBRANGING)
REQUIRED ONLY FOR WIDE INPUT BANDWIDTHS
— SOME A/D HAVE T/H OR S/H BUILD-INTO THE PACKAGE
— REFERENCE IS BUILD-IN
— INPUT VOLTAGE IS PROGRAMMABLE
— HAS A BUILD-IN INPUT AMPLIFIER
SLOW SPEED ACQUISITION
(BELOW 200 KHz)
INPUT ANALOG VOLTAGE
A/D
FEEDBACK (SERIES-SERIES PARALLEL)
SUCCESSIVE APPROXIMATION
— REFERENCE IS BUILD-IN
— INPUT VOLTAGE IS PROGRAMMABLE
— HAS A BUILD-IN INPUT VOLTAGE AMPLIFIER
— HAS A BUILD-IN S/H (IF NOT EXT. LOW SPEED S/H ARE DESIRABLE)

FIGURE 2.2.19 SPEED VS. DRIVER REQUIREMENTS

selecting an input amplifier with its roll off point at or near the Nyquist frequency is a mistake. Phase becomes non-linear in most amplifiers at greater than one-third to one-half of the 3 dB bandwidth. Group delay is therefore not constant and harmonics are delayed unequally. The net result is distortion, and degradation of the system's ability to accurately convert signals. Thus it is important to maintain amplifier bandwidth of at least three times the Nyquist rate to minimize gain and phase aberrations. Then, the anti-aliasing filter can be designed independently from the less precisely controlled transfer function poles of the amplifier.

2.2.5.2.2 Driving Capacitance

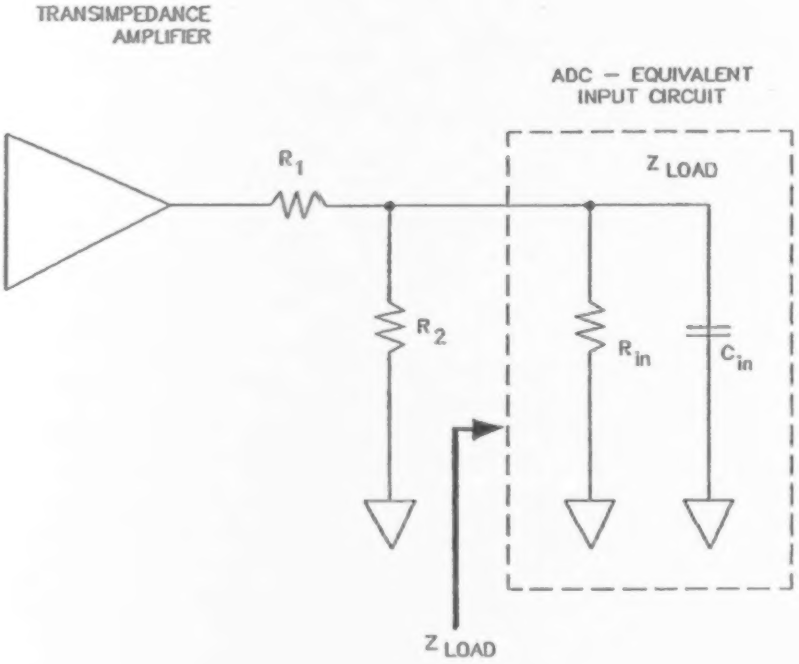
In a parallel converter the transimpedance amplifier must drive a non-linear capacitance in parallel with non-linear resistance. This nonlinearity is due to the dramatic changes possible in the input impedance characteristics of the comparators, depending on whether they are in their on or off state.

To minimize the consequences of changing capacitance, the transimpedance amplifier must have a fast settling time, wide bandwidth, a high slew rate, and low output impedance.

Experiments have shown that the circuit in Figure 2.2.20 will provide maximum bandwidth, flatness, and settling time when driving capacitances of up to 300 pf.

Resistor R_2, placed in parallel with the input impedance of the converter, should be chosen so that $R_2//R_{in}$ equals about 50 Ohms. This helps to keep the RC time constant low and associated bandwidth high (see example given in 2.2.4.2.3). It also helps to minimize variations caused by changes in R_{in}.

When placed between the output of the amplifier and the converter, R_1 serves to isolate the input capacitance C_{in} from the amplifier. This cuts down amplitude peaking. Although the optimum



$$|Z_{LOAD}| = \frac{R_{in}}{\sqrt{1+\left(\frac{W}{W_o}\right)^2}}$$

where: $W_o = \frac{1}{R_{in} C_{in}}$

C_{in} is fixed

R_{in} can be affected by R_2

therefore:

$$W_o \propto \frac{1}{R_2 // R_{in}}$$

FIGURE 2.2.20 TRANSIMPEDANCE AMPLIFER CONNECTED TO ADC

value of R_l depends on converter parameters, the curve of Figure 2.2.21 gives a good first approximation.

2.2.5.2.3 Settling Time

For A/D conversion of pulse waveforms, settling time of amplifiers and T/H or S/H is an important measure of waveform reproduction fidelity. These components must be able to settle to within 1/2 LSB of the correct value within the sample period allotted.

Figure 2.2.22 illustrates settling time available versus sampling frequency . As an example, consider an 8-bit 100 MHz flash A/D converter, a settling to 0.2% within 10 usec is necessary. This is a stringent requirement, but unless it is met the full capabilities of the flash A/D converter cannot be realized.

2.2.5.2.4 Slew Rate

Another consideration is the slew rate of the drive circuitry. The maximum slew rate for a sine wave is:

$$\frac{dV}{df} = 2\pi f_{in} A \quad \text{Volts/sec.} \qquad \text{eq. (12)}$$

Therefore, to digitize a 5 volts peak sine wave at 20 MHz, a slew rate of 630V/usec is needed. It is always a good idea to use an amplifier with much higher slew rate than that actually needed, because once an amplifier comes close to slew rate limiting, it becomes highly non-linear and fails to settle properly. Figure 2.2.23 illustrates slew rates required as a function of maximum frequency in the bandwidth for different amplitudes of signal.

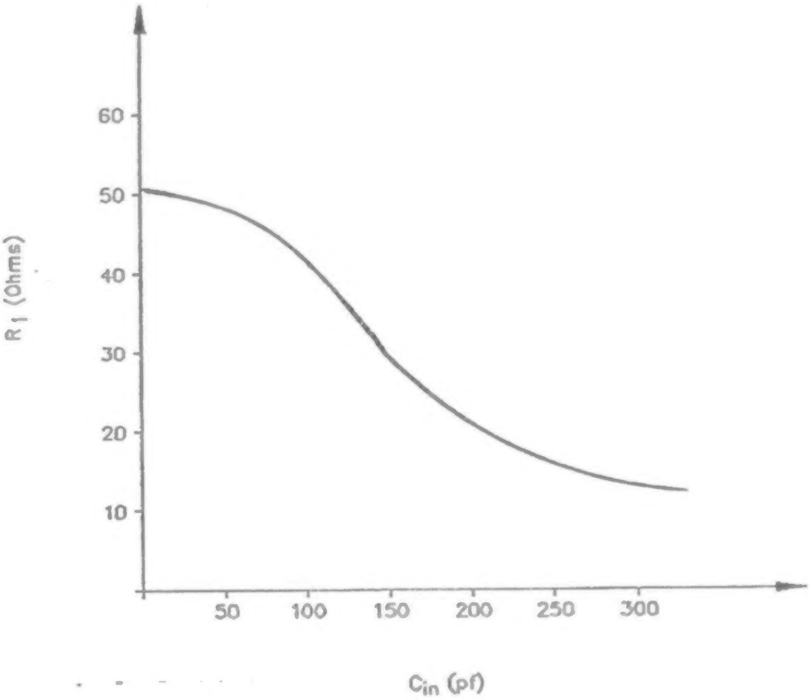


FIGURE 2.2.21 WHEN THE AMPLIFIER DRIVES CAPACITIVE LOADS, RESISTOR R_1 IN FIGURE 8.0 ISOLATES IT FROM THE INPUT CAPACITANCE, C_{in} THIS CURVE WILL GIVE A GOOD FIRST APPROXIMATION FOR VALUE OF R_1. THE OPTIMUM VALUE DEPENDS ON SEVERAL FACTORS.

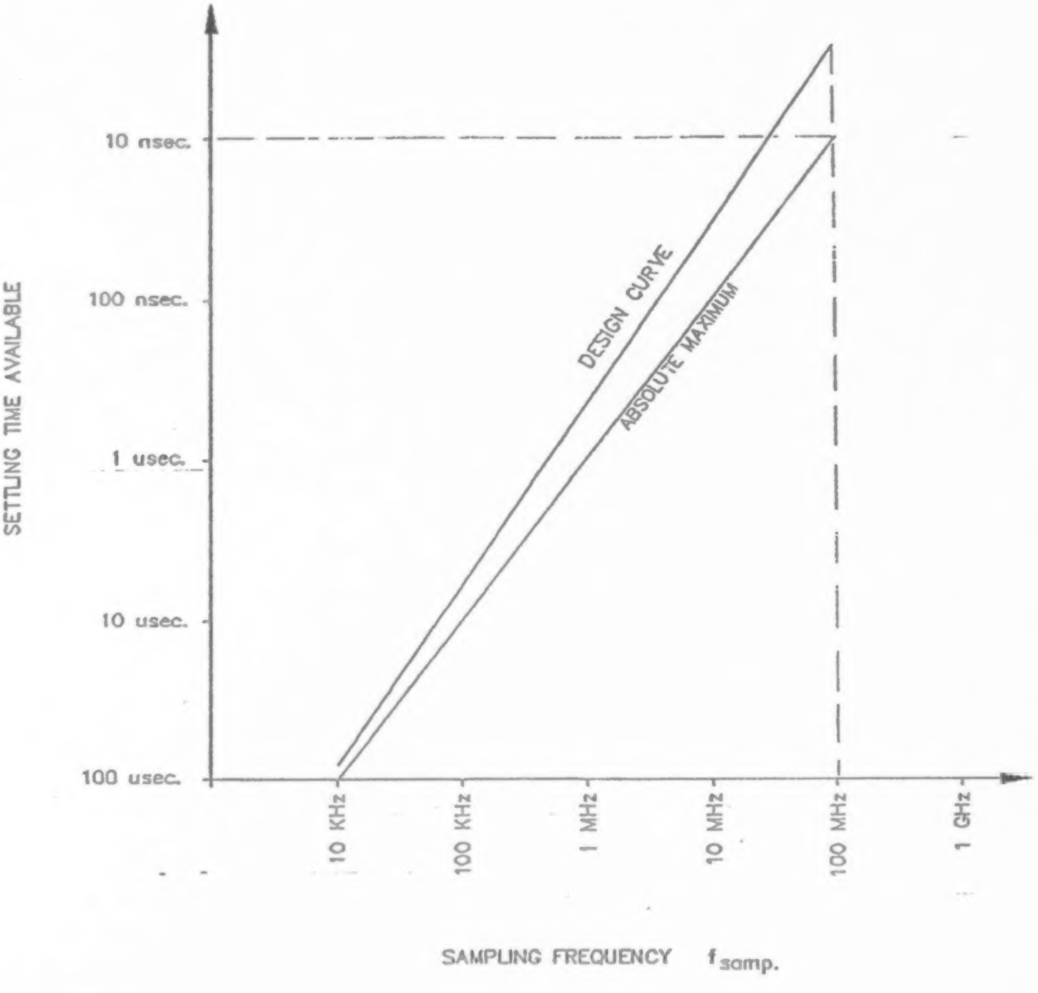


FIGURE 2.2.22 SETTLING TIME VS. SAMPLING FREQUENCY

SLEW RATE → $\frac{dV}{dt} = 2\pi f_{in} A$

A = maximum amplitude of signal

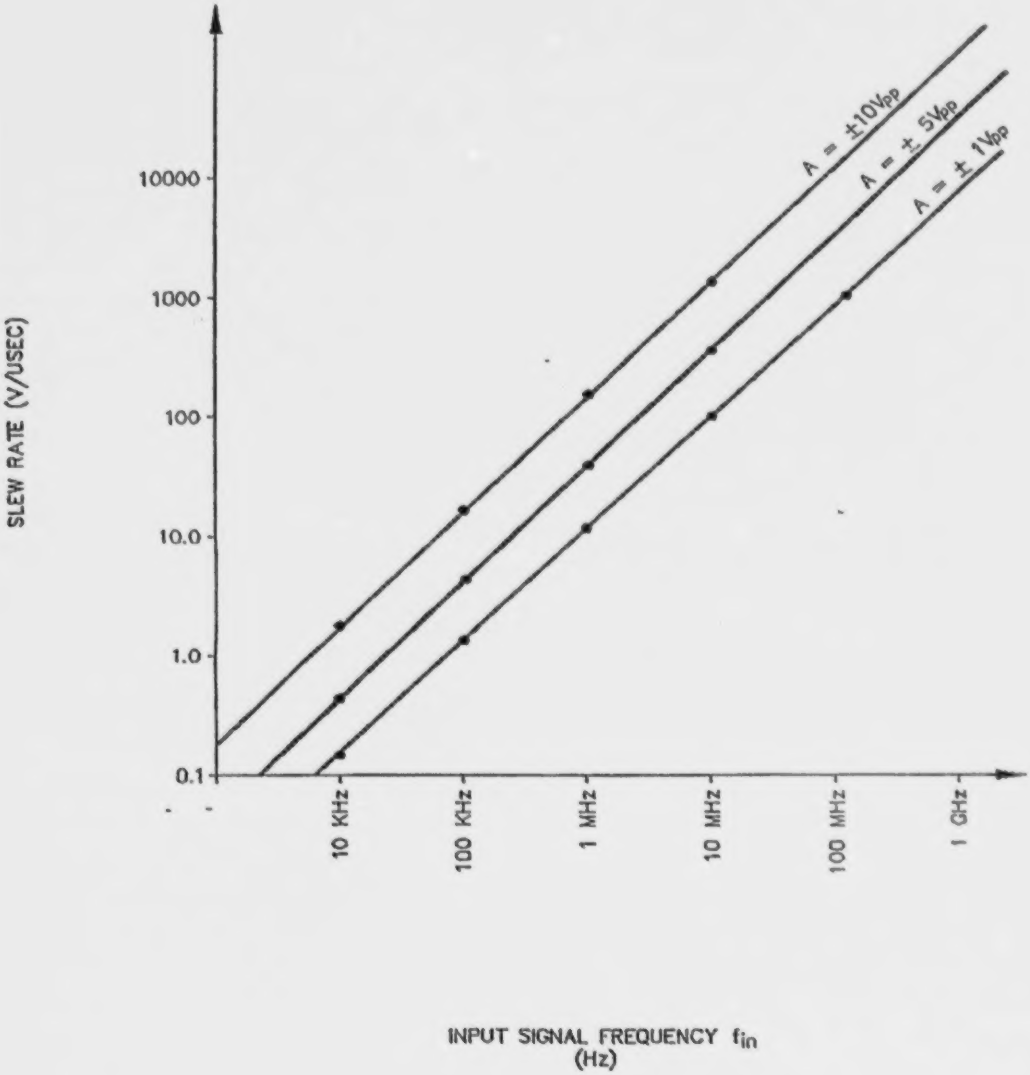


FIGURE 2.2.23 SLEW RATE AS A FUNCTION OF FREQUENCY

2.2.5.2.5 Distortion, Noise and Amplification Fidelity

All the manufacturers of transimpedance amplifiers supply a set of specifications in terms of graphs from which a great deal of data is obtained describing the performance of the device under various operating conditions. Some of these graphs are illustrated in Figure 2.2.24 (a) and (b).

The graph of intercept point versus frequency, Figure 2.2.24, makes it easy to predict the distortion at any frequency, given the output voltage of the transimpedance amplifier. First convert the output voltage V_0 to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P=(10\log_{10}(20\ V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, the second harmonic will be $S_2 = (I_2-P)$ dB below the level of P. The third harmonic will be $S_3 = 2(I_3 - P)$ dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression level.

Approximate noise figure can be determined using the Equivalent Input Noise graph on Figure 2.2.25. The following equation can then be used to determine noise figure (F) in dB.

$$F = 10\log_{10}\left[1 + \frac{V_n + \dfrac{i_n^2\ R_F^2}{A_v^2}}{4KTR_s\Delta f}\right] \qquad \text{eq. (13)}$$

where V_n is the rms noise voltage and in is the rms noise current. Beyond the breakpoint of the curves (i.e. where they are flat), the broadband noise figure equals the spot noise figure, so Δf should equal one (1) and V_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and f set to the appropriate bandwidth.

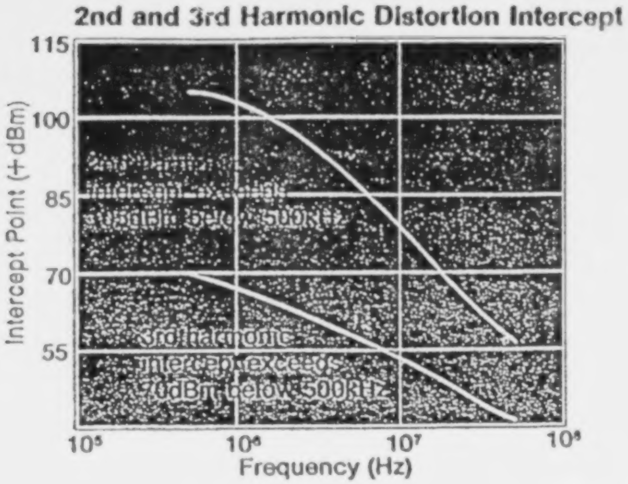


FIGURE 2.2.24 a) SECOND AND THIRD HARMONIC DISTORTION INTERCEPT

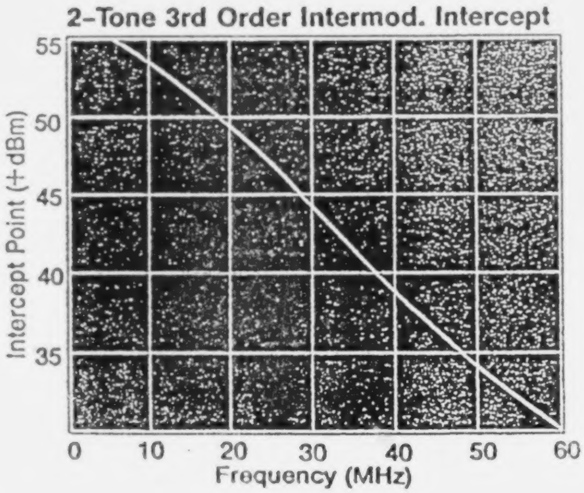


FIGURE 2.2.24 b) 2-TONE AND THIRD ORDER INTERMOD. INTERCEPT

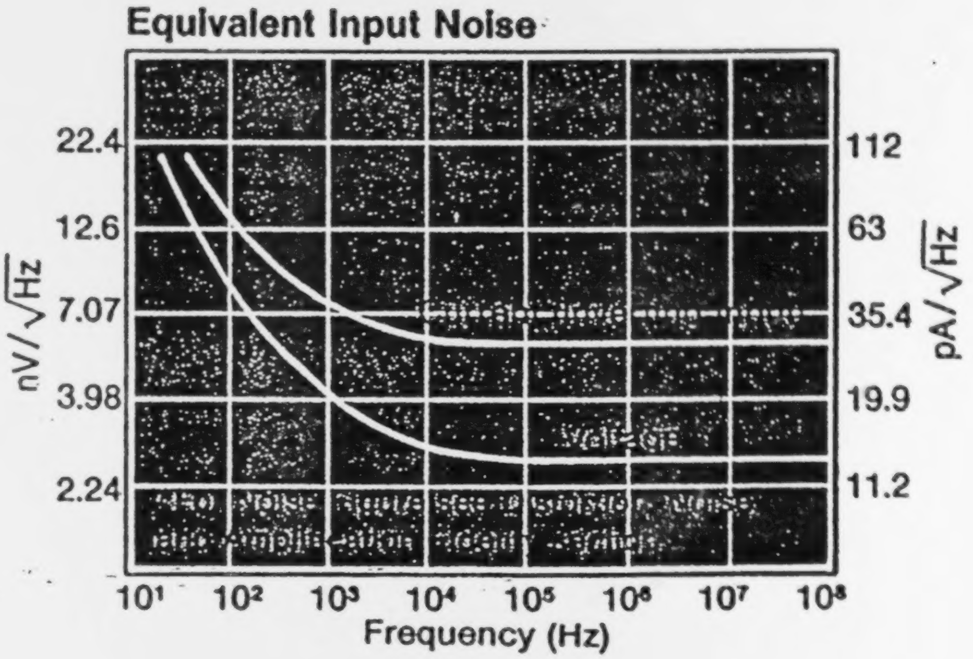


FIGURE 2.2.25 TYPICAL NOISE FIGURE DATA OF A TRANSIMPEDANCE AMP.

2.2.5.2.6 Conclusion

High speed data acquisition requires the most advanced transimpedance amplifiers available in the market today. When a high speed "flash" converter is used to digitize analog signals, a transimpedance amplifier placed between a T/H and the A/D becomes essential in order to drive the highly dynamic input impedance of the converter.

In this analysis we saw that some parameters such as settling time and slew rate are critical when selection of an amplifier is to be made. Therefore, in order to achieve optimum performance in a digitizing system, the value of these parameters should be chosen very carefully.

Finally, cost of these devices varies according to drive capability, that is, the higher the signal frequency they can drive the more expensive the device is.

Table 2.2.11 shows a survey of some of the most advanced transimpedance amplifiers currently available on the market.

2.2.5.3 Driver Trade-off Considerations

To conclude this section, a few recommendations on how to select the proper drivers should be made.

In the case of T/H or S/H devices, the parameters described in the analysis should have maximum errors not exceeding those listed in Table 2.2.9.

Also, the maximum sampling speed of the device should be chosen at least 20 to 30% higher than the actual sampling speed of the A/D. This is to prevent longer settling times introduced by unexpected loading at the output of the device.

TRANSIMPEDANCE AMPLIFIERS	SLEW RATE (V/usec)	BANDWIDTH (full power)	SETTLING TIME (nsec.)	OUTPUT (Volts, Current)
ANALOG DEVICES AD 9610	3500	92 MHz	18 ± 0.1%	± 12 V. ; 50 mA
COMLINEAR CLC-220A	7000	100 MHz	15 ± 0.02%	± 12 V. , 50 mA
COMLINEAR CLC-203A	6000	60 MHz	15 ± 0.2%	± 11 V. , 100 mA
COMLINEAR CLC-221A	6500	130 MHz	24 ± 0.05%	± 12 V. , 50 mA
HARRIS HA-5033	1300	65 MHz	50 ± 0.1%	± 10 V. ,100 mA

TABLE 2.2.11 LIST OF SOME STATE-OF-THE-ART TRANSIMPEDANCE AMPLIFIERS

Linearity of the device should not change more than ±1/2 LSB (Table 2.2.9) throughout the temperature range of operation. Note that some of these devices dissipate large amounts of heat especially diode bridge T/H, therefore a large temperature change might affect the linearity error.

The input and output impedances should be selected such that their effect causes minimum loading conditions to the pre-amplifier and post-amplifier.

In the case of transimpedance amplifiers, a selection should be made such that a device having a slew rate 20 to 25% more than required, in order not to cause excessive settling time, is chosen.

If digitization requires conversion of pulsed signals, choose a settling time such that the combined total of settling times on the analog path is less than 80% of the actual signal pulse width.

An amplifier full power bandwidth should be at least three times the Nyquist rate to minimize gain and phase aberrations.

2.2.6 Digital Interface Considerations

Regardless of the type of A/D used in the final system configuration, the means to transfer the converted data to a storage medium for further processing, is dependant on the system requirements as a whole.

Specifications defining system throughput, bandwidth, quantization level, pulsed or CW environments, size and power availability, all dictate the form of the A/D interface to the outside world.

Most interfaces are designed to incorporate a composite of each of these issues in a prioritized fashion. These compromises are weighed in accordance with their importance to the overall system performance requirements.

The following presentation will review the various types of architectures and be viewed in terms of their advantages and disadvantages, given that the system specifications are defined as the analysis proceeds.

This type of pro and con discussion lends itself to be graphically presented. But in so doing many details can be left out. Therefore the descriptions for this portion of the discussion will be dealt with in narrative form.

2.2.6.1 Interface Architectures

NOTE: When discussing series/parallel architectures, it must be made clear here that no confusion exist between the definition of series/parallel type A/D converters and series/parallel forms of A/D interfaces. The text contents here will deal with the interface forms, and not the A/D type. For description of the latter, refer to Section 2.2.4 of the report.

Certain interface architectures are more appropriate to high speed type converters where bandwidth is of prime concern, than high multi-bit slower converters, where high dynamic range and resultant quieter noise floors is of main importance.

The series approach can be used by almost any type of converter interface, because of its straight forward design philosophy. Whereas the parallel and its sub-structures: pipelined overlapped, and cache, are principally used to enhance overall system bandwidth.

The following descriptions of each interface type will be reviewed in terms of the principle characteristics of speed and bits.

2.2.6.1.1 Series Circuits (Speed)

Sometimes referred to as the "brute force" method. So named because of its relative simplicity and maximum clock rate design. The front-end circuits are all clocked at the maximum rate and only one set of processing circuits are required to achieve the end result, see Figure 2.2.26. This type of approach has good system throughput, can occupy relatively smaller real-estate and usually no sample and hold is required if the flash type A/D is used (the "series/parallel type A/D will always require a sample and hold due to its design nature). As a consideration to the latter advantage, current A/D's have quite a good input analog bandwidth with respect to its sampling rate, thus allowing paralleling of A/D's provided the front-end has enough bandwidth and its combined input capacitance is low enough. But not to dwell on this extensive topic, the absence of a S/H adds to the attractiveness of the "brute force" concept.

But aside from this short list of advantages, it suffers from some key disadvantages namely, and most important, the design is limited by the state of the technology with regard to limits in sampling rates. If the kernel in a system specifies an N bit system whose bandwidth requirements exceeds what is available, the series approach will fall short of its goal without incorporating some form of paralleling.

There is a subtle means however where one can cheat by using two series circuits in quadrature at the RF level by using a quadrature mixer to overcome this problem see Figure 2.2.27. Even though this can be considered a form of paralleling,it is not in the form as defined in the coming chapters.

A second negative trait is that if any writable interface is accessed by the converter, it must be as fast as the A/D conversion rate and large enough in capacity to store all the information the

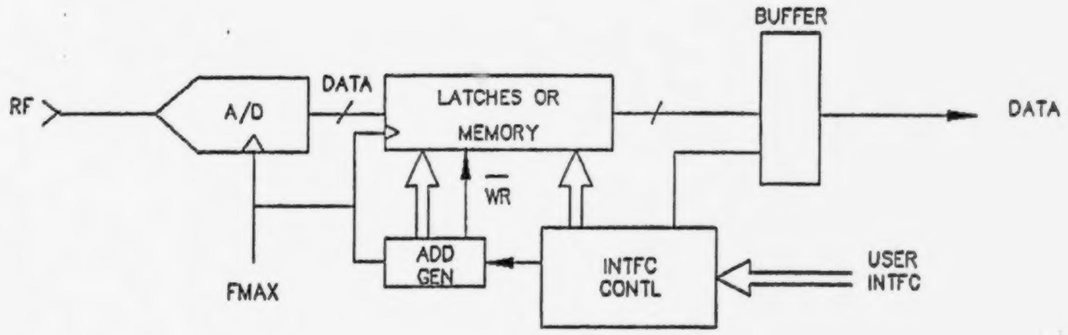


FIGURE 2.2.26 SIMPLE SERIES FRONT END

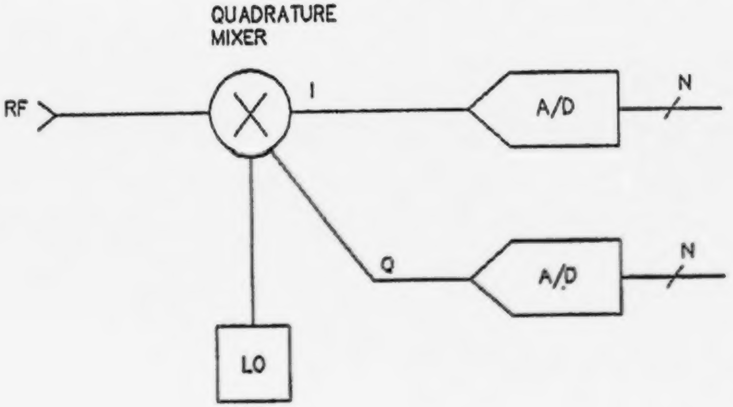


FIGURE 2.2.27 DOWNCONVERSION AND MIXING FOR I AND Q

application requires. This can result in a memory block that can be very large and consequently very power hungry.

The memory speed issues can be dealt with by adding in a serial to parallel conversion scheme where the converter data is delayed by N shifts prior to data storage, as shown in Figure 2.2.28. By having N stages of serial shift, the addressing rate drops by $n(1/f_{s})$, where n=num of stages and f_s=sample rate. This allows for lower memory cycle rates, thus the use of denser memory chips, since cycle time is directly related to memory size (the longer the access time the deeper and wider the memories available).

The parallel conversion scheme gives up data throughput time advantage, since the output data will not be available for N shifts.

The quadrature down conversion scheme requires extra real estate due to the additional data converter with its support circuits and has serious circuit balance problems which grow more severe with sampling rate and the number of bits.

2.2.6.1.2 Series Circuits (Bits)

Cases where a high dynamic range is required and bandwidths are not the prime issue, the implementation of 10 to 18 bit converters are readily available. The critical specifications of a low SNR and therefore yielding a high effective bit system over most of the usable bandwidth, bring with it a subtle change in design philosophy.

The series method at lower clock rates open the doors for less elaborate type of A/D interfaces. Depending on throughput, memory size requirements or the need to manipulate stored data, the A/D can be interfaced directly to either dual port memories or FIFO type structures.

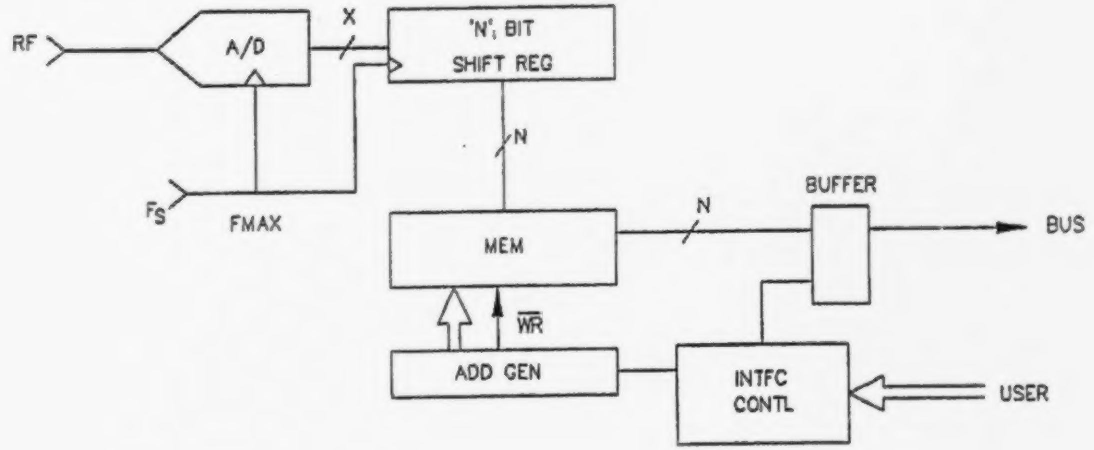


FIGURE 2.2.2B MEMORIES IN SERIES METHOD
METHOD TO ALLOW FOR DENSER

Dual port random access memories (DPR) and FIFO's both share the same trait of providing the means to asynchronously read an internal memory cell while currently writing in the same or another cell. This allows for throughput in real time. The main difference is that the DPR structures require a more elaborate addressing scheme, than the simple two-wire handshake that FIFO's offer. The DPR designs though, have random access capability and the data is always resident, unless it is overwritten. Unlike the DPR, the FIFO has sequentially timed access and the data is available only once when read and is lost forever. This weakness can be overcome at the expense of additional circuitry, but it must be weighed against what the DPR designs offer in equivalent performance. For simple efficient designs however, FIFO's are a good design alternative.

While high speed designs target low spurious performance, as well as low speed 12 or 16 bit designs, they are theoretically limited by the approximate 6 dB/bit rule, and thus system designers are forced to give up spurious performance for bandwidth. The resultant interfaces are designed to accommodate speed and dynamic range within the technological limits of the chosen hardware.

High dynamic range A/D's require interfaces and layout techniques to minimize the noise contribution and thus keep the integrity of the sampled signal as uncorrupted as possible. Multilayer PCB's providing low impedance power and ground plains, coupled with selected guard areas, and EMI and RFI shielding techniques all contribute to the maximizing of signal integrity. But the A/D, being monolithically constructed, shares both the analog comparators, in the case of a flash type A/D, and the potentially noisy world of the digital encoder and drive logic, on the same substrate. Hybrid type A/D's offer some isolation in these areas, but cost, power consumption, multiple supplies and real-estate may be inhibiting factors in choosing them.

Once the digital switching waveform is available at the output port of the A/D, the data must be passed on to the interface circuitry. In so doing, electrically, the A/D and the interface circuits, which share the same power and ground planes, shift potential due to current loading and mismatch effects and can corrupt the sampling process at the sensitive analog front end. Despite attempts at decoupling and shielding, the fast rising edges of A/D outputs contain many harmonics that can couple and radiate to adjacent signal paths. In addition, the fast rising edges demand instantaneous current from the decoupling capacitors to satisfy the V_{OH} and V_{OL} requirements. This transient effect can cause power supply drops and peaks and ground potential elevations enough to cause equivalent LSB's to be distorted.

A 16 bit A/D with between a 2.5 to 10V reference has an equivalent of 3.8 to 15.2 mV/LSB sensitivity. If the ground plane deviates by a multiple of this parameter with respect to its reference, it can be seen that the 16 bit converter really is a 12 to 14 bit converter. Of course other factors also present a degradation of the effective bits but these are discussed elsewhere in this report.

A method to isolate the ground plains is available to off load the heavier digital transient producing circuits from the sensitive analog comparator and reference circuits. By using appropriate opto-isolators in the digital path and separating the ground planes on the PCB, the transient disturbances of the digital switching are effectively kept away from the analog power and ground plains of the analog circuits.

It is also recommended that separate linear supplies be used for both the digital and analog power sources. Switching supplies have incidental switching regulator noise components on top of its DC output. For example, with 12 or 16 bit converters, once the signal has been digitized the power supply switching sidebands would be very apparent in the resulting FFT.

The effects of ground loops in the final system should be avoided. In the obsession of ensuring adequate grounding, the appearance of ground loops which cause noise, can become a problem if the system is choked with ground wires to the power supply. To avoid this problem, all grounds should be terminated at one point, no matter what its current carrying ability. This forces balanced return current to each supply and prevents switcher noise from corrupting the line supplies. Return lines should be twisted to reduce the size of the effective loop antenna formed by the power supply wires. Typically on a multilayered PCB, exhibiting separate digital and analog ground plains, they are connected together at the edge connector and then terminated onto the power supply individually. Figure 2.2.29 illustrates this technique.

2.2.6.1.3 Parallel Circuits

Some of the shortcomings of the series method can be overcome by incorporating a multiple of series circuits running at lower clock rates. The circuits are paralleled and effectively the signal is sampled in an interleaved fashion resulting in each digitizer under sampling the signal by taking every N^{th} sample, depending on the number of digitizer channels (N), Figure 2.2.30. This can yield an effective sampling rate, and thus bandwidths, much higher than a single series channel can achieve. Also, due to the lower clock rates, slower more dense memories can be used resulting in the ability to store longer RF information. Additionally, by the application of the serial to parallel conversion method to each channel, considerable memory depth can be attained.

Referring to Figure 2.2.30 (a), the digitizer channels are all connected to a common RF source. The system clock however is time staggered or phased according to the number of channels. If each A/D is capable of sampling at F_s and the required digitizing bandwidth is BW then the number of channels N is defined as:

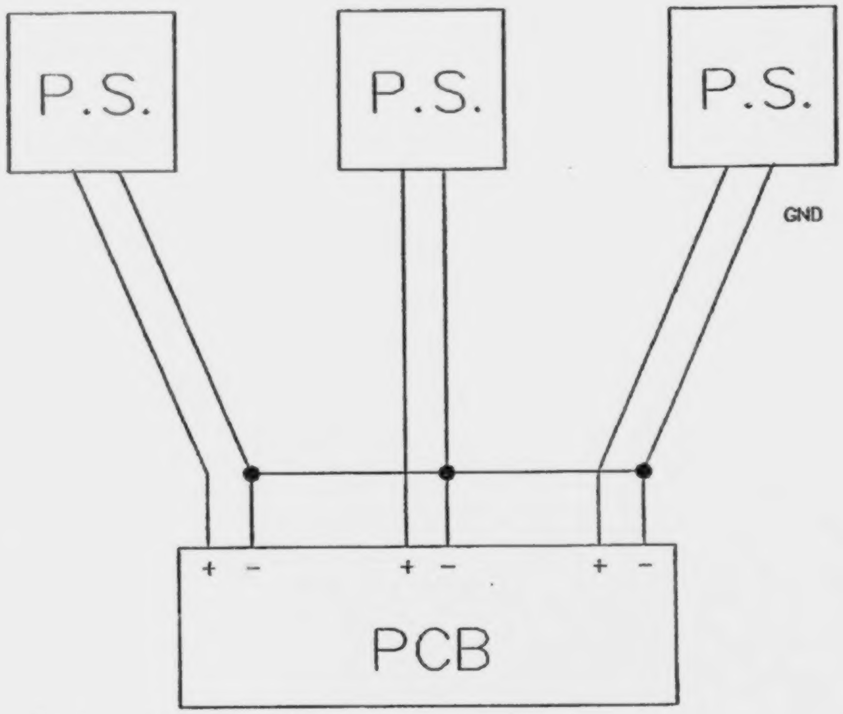


FIGURE 2.2.29 GROUND DISTRIBUTION

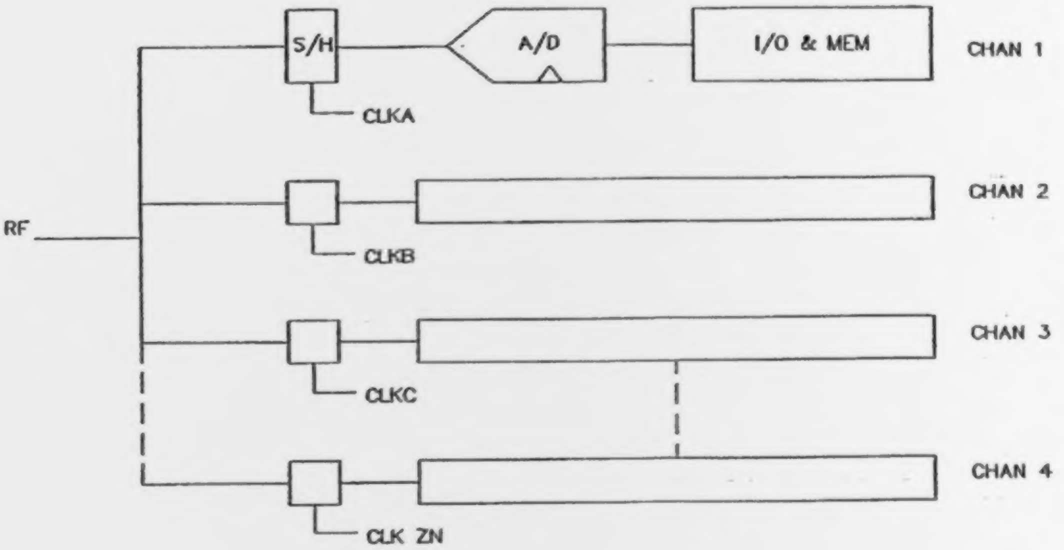


FIGURE 2.2.30 (a) PARALLEL DIGITIZER USING PHASED CLOCKS

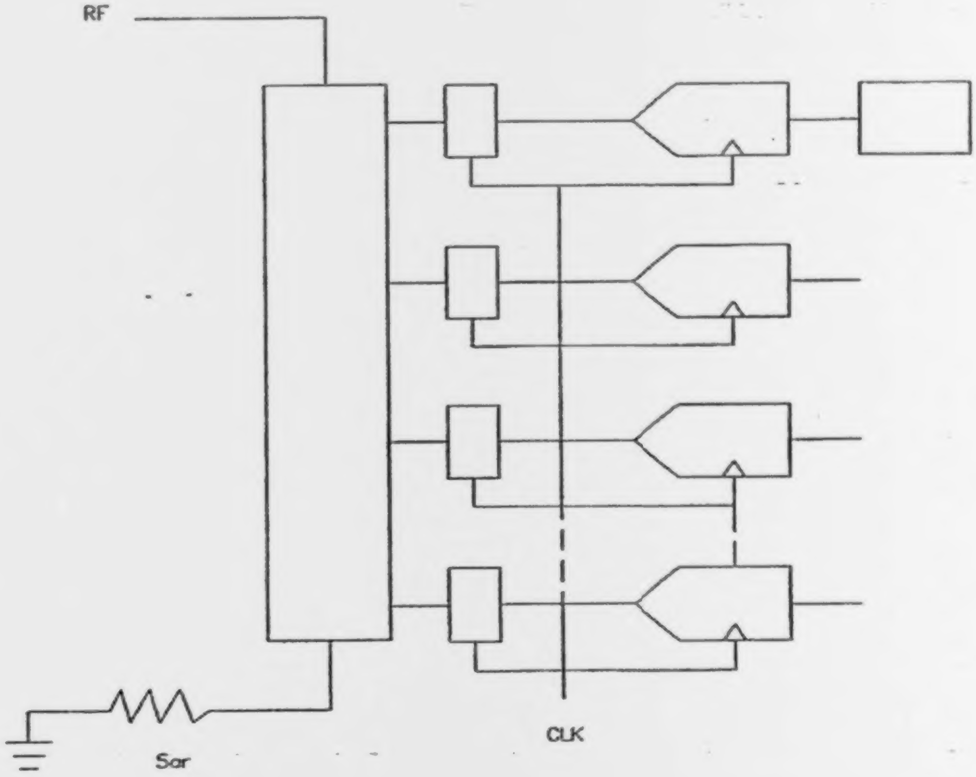


FIGURE 2.2.30(b) PARALLEL DIGITIZER USING RF DELAY LINE

@ Nyquist $2F_s = BW_s$ eq. (14)

therefore $N = 2BW_s \times \frac{1}{F_s}$ eq. (15)

therefore the phase angle offset for each channel is

$P.A. = \frac{360^{\circ}}{N}$ eq. (16)

One large disadvantage to the clock phasing approach is that individual timing circuits are required for each channel because of the nature of overlapped timing, thereby compounding an already heavy component count and thus power burden.

Depending on the number of parallel channels and the timing spread from the first channel to the last channel, a method to reduce the timing burden can be used. Once the overlapped data is available, the RAM banks for each individual channel can be clocked all at once by using Registered Rams. This results in one set of timing circuits for all the RAM banks. Of course appropriate precautions must be considered in the light that many loads are driven at once, and its impact in terms of transmission line distortions and power supply decoupling ability.

Another alternate way to ease this problem is to time delay the RF signal in much the same manner as the clock network, but by using an RF meander or delay line, Figure 2.2.30 (b), rather than a digital delay using shift circuits. The calculations previously reviewed are equally as valid to determine the line characteristics. The calculations would effectively produce an equidistant fixed delay line at each tap interval. The clocks can now be connected together and thus allow only one set of timing circuits. It can be viewed as a form of serial to parallel conversion at the RF level. A prime disadvantage of this approach however is that the design has no flexibility in tap spacing adjustment. This inability to 'Fine Tune' the line results in sampling errors, which in turn produce spurious signals in the final spectrum. These types of errors can be minimized by characterizing all sources of error and adjusting the delay line parameters where necessary.

Both concepts must incorporate a sample and hold circuit due to the inability of each digitizer to handle the high input slew rates present at its input node. The S/H would provide the necessary input characteristics, hold and drive capability to its adjacent A/D, thereby insulating the A/D from what can be potentially devastating conversion results.

A unique characteristic of this approach is that each A/D, being an agent of undersampling, traverses a DC to Nyquist course and back to DC. Depending on the number of channels and the sample rate, each sampler can sample from DC to Nyquist many times over the designed bandwidth.

This type of polyphase environment can yield good results provided these precautions are adhered to:

a) Careful meander line design - equal tap spacings
  - identifying all sources of error

b) Master clock stability

c) S/H design.

Each of these considerations if not adhered to properly can produce an undesirable spectrum, with many spectral products destroying the SNR and thus the effective bit performance.

These points will not be dwelled upon however, since they have been discussed in detail in previous sections, suffice to say that solutions exist to alleviate these problems and these will be addressed in subsequent sections.

If this type of architecture were to be used, the incorporation of gate arrays should be strongly considered to alleviate the increased component counts due to channel replication and thus serve to reduce system complexity and enhance system reliability.

In cases where parallel architectures are required but cannot accommodate gate array technology because of cost, time or manpower restrictions, there is an alternative. The pipelined overlap approach can provide performance enhancements in the areas of fast throughput and provide a simple timing and control interface, since it directly interfaces to the output ports of the A/D, see Figure 2.2.31.

Pipelining is defined as the ability to process data in one part of memory while data acquisition is still taking place in another part of memory. This technique allows for post processing on-the-fly if it is designed with this requirement in mind.

Even though this approach can be categorized under series circuits, highlighted earlier, it does have some subtle differences, putting it in a class by itself. A few distinctions are that coupled with the integral cache RAM, it can store data in a longer string than a shift register can, thereby decreasing the number of pipeline elements. Also, it can continually process data depending on memory size and processing time windows, and therefore memory size does not become an issue since the available memory is utilized very efficiently.

It can be described such that the A/D data gets written into cache RAM A, taking up time T. Once RAM A is filled, the control interface channels the A/D data to cache RAM B. While B is filling up A is emptied to the post processor buffer at a slower rate. This time to empty A is equal to the time to write to N pipeline elements x its memory size x writing speed, minus the time to fill one array.

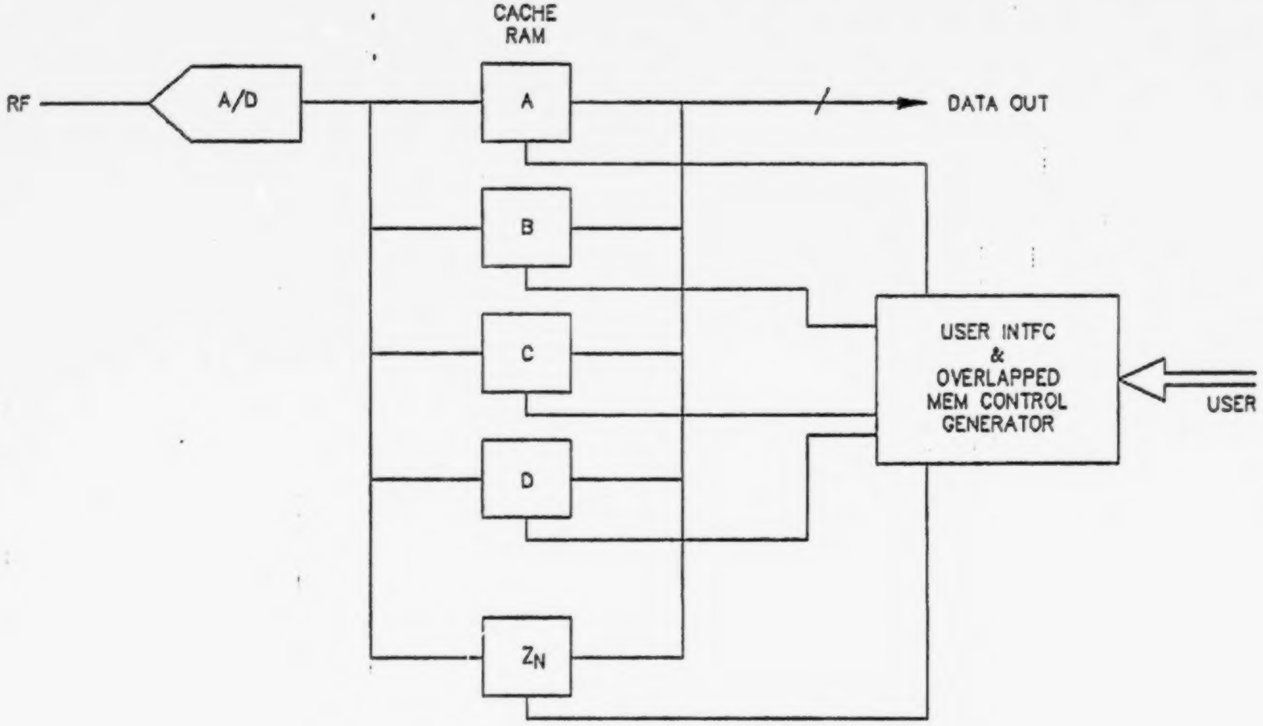


FIGURE 2.2.31 MEMORY STRUCTURE

ie. $T_s = (N \times \text{Mem size} \times t_a) - (\text{Mem size} \times t_a)$ eq. (17)

This is because the time to write to any one array must be cancelled out from the total read time. Once B is full it waits to be read, since A is still being dumped. Memory C now begins to fill. This stepping process continues for all elements of the array until A is finished reading, and is ready to be written to. Once A begins to write again the remaining elements are either waiting to read out or in the process of being read out. Since the cycle is unbroken, this process can continue for the longest RF pulses, CW or necessary FFT sample size.

To facilitate maximum performance at very high speed the A/D can be interfaced directly to GaAs memory parts. If the requirement is a lower speed 10 to 16 bit unit, the cache elements can be FIFO's or dual port memories.

2.2.6.1.4 Parallel Circuits

When the need is to increase the quantizing level but at the same time not sacrifice bandwidth, there is a means to extract this requirement. All A/D converters require some form of reference voltage, whether it is internally generated or externally available. By adding a new external reference chain, where each A/D is attributed a portion of the new reference voltage, essentially equivalent to each individual A/D maximum reference voltage, the combined action yields the desired result. This external chain is similar to the internal voltage divider network found in the reference ladders adjacent to flash converter comparators. Effectively each A/D converts a portion of the input signal, and the resultant digital information is wire or'd via the overflow of each successive A/D, to yield the extra data bits. See Figure 2.2.32.

There is one main problem with this approach. The A/D's selected for this task must have much less than 1/2 LSB linearity

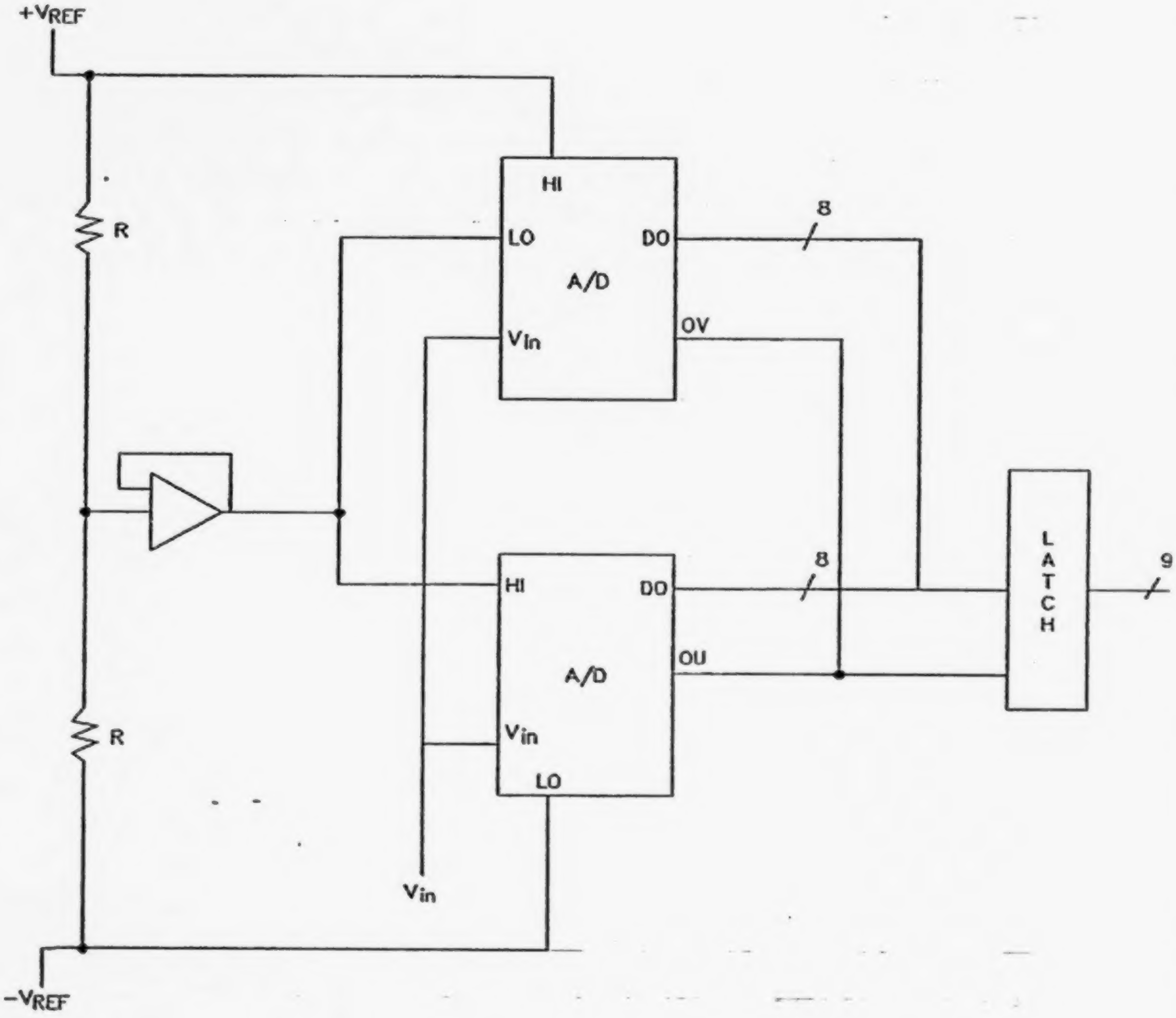


FIGURE 2.2.32 A/D'S PARALLELED FOR MORE BITS

error. The act of combining A/D's in this manner does not mean the linearity error of each A/D is independent. Essentially the linearity error of each A/D can be summed, and if the result is approaching 1 LSB or greater, the net effect will yield no performance increase.

For example, in the case of paralleling 2 A/D's the linearity must be better than 1/2 LSB. For paralleling 4 A/D's, to yield two more effective bits, the error must be much better than 1/4 LSB. The overall gain of using this method can only be realized if the combined linearity error remains at about 1/2 LSB.

2.2.7 Bus Architectures

Of the many established buses available today, some, if not all the characteristics of these buses may be of any use in some systems. Some application specific systems require the design and support of a custom bus architecture to minimize the control protocols, and thus enhance the efficiency of data transfer. On the other hand the use of a bus which is universally recognized can be a great asset due to its support and products base, even though in the end, some lesser version may be used as a system compromise.

Reviewing the needs of this study, it is not overly apparent what the performance requirements are, but for the sake of system efficiency, usually data transfer speed is of highest priority. Ignoring the control protocols of the VME bus format, this bus architecture seems to be the closest to the needs of this system. It has a wide parallel data path, and can address large off-board memory blocks, and its control protocol is relatively easy, since the bus philosophy was developed to cover a wide range of applications.

If the system requires a higher throughput than the VME hardware can support, then a custom bus may have to be developed.

Typical VME transfer rates with a 32 bit bus and custom bus controller circuitry can output up to 40 MBPS.

The other communication buses, IEEE 488, RS-232C, RS-422, 1553, SCSI, do not exhibit the traits needed to satisfy the data form and speed.

2.2.8 Practical Interfacing Considerations

Best performance is only achieved when accepted design standards are strictly applied. They must include layout considerations covering transmission line rules, whether they are stripline or microstrip choices, ground and power planeing, noise guards, EMI, RFI shielding, appropriate common sense component placement, and proper component selection in terms of desired performance in the form of package style and mounting techniques. Each of these rules can only slightly be compromised because of cost restrictions or size limitations. For the most part however, a priority must be placed on these standards to get maximum results.

If reliability is to be considered high on the priority list, component count, its qualification standard and system operating temperature must be input into the equation before the design begins. Simplicity in design at the expense of perhaps some bells and whistles, will certainly increase reliability. Using military qualified standard parts whose functions are tested over military temperature ranges will also enhance reliability.

When high speed components are used, and the transmission lines are relatively long (>2" at 300 MHz or above), it is recommended that the line not only be 50 Ohms but be differential wherever possible. When driving multiple loads from one source, the transmission line should be terminated just beyond the last load. The number of ECL loads should be less than ten. Above ten loads VSWR effects occur, along with rising edge degradation which may be unacceptable. Rather then repeating what are accepted standards, the reader is referred to a more detailed description of high speed design rules which can be found in the Motorola, Fairchild or Signetics ECL design manuals.

High speed A/D's will always have a separate power and ground connection for the digital and analog supplies. When layout proceeds, ensure that space is provided for allowing adequate decoupling of each supply using high frequency capacitors whose series resonance is close to the operating sampling frequency. This ensures a non-reactive ground for unwanted sampling transients. There should be a series of capacitors in parallel to each supply, including RF ceramic and tantalum types allowing different parts of the unwanted spurious spectrum to be bypassed effectively to ground.

Depending on current requirements to the load, small chip inductors can be added in series to the supplies to further reduce unwanted spurious signals and noise.

In the case of high bit count A/D's, in the order of 10 to 18 bit A/D's, the overwhelming precautions to be addressed are those that insulate the A/D from noise in the sensitive front-end. The choice of opto-couplers, as was discussed earlier, should be considered, if not mandatory. Because A/D's of this nature are normally the low speed variety, in the order of 40 KHz to 10 MHz the choice and form of the sample and hold is very critical. The hold/droop specification has a direct impact on the dynamic range and effective bit performance. If the holding function is not adequate, the uncertainty of the aperture jitter specification will destroy the ability of the A/D to provide for its designed purpose. The generation of spurious signals is directly related to the amount of average voltage variation while the aperture window stays open. If the droop is excessive, the delta V over delta t_a ratio would produce a proportionally corrupt output spectrum (Figure 2.2.33). But if the hold function is flat with no droop,

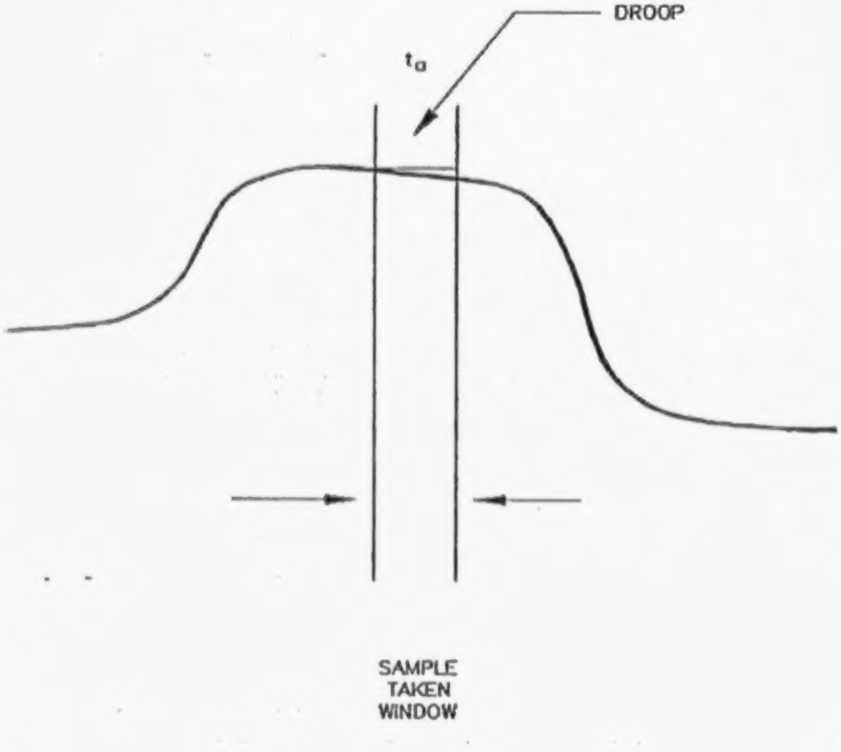


FIGURE 2.2.33 DROOP CHARACTERISTIC DURING SAMPLE WINDOW

the A/D will have a much easier time sampling this held signal and thus produce a high quality output result.

2.3 Digitization

Digitization is a process in which an analog signal is converted to a discrete digital time signal. This enables powerful "Digital Signal Processing" (DSP) techniques to be applied by means of fast computers or dedicated processors to extract as much information as possible from the original signal.

Three different areas of the radio frequency spectrum are examined, to assess the feasibility of current technology in obtaining the best possible digitization of an analog signal while maintaining the features of a good surveillance receiver.

2.3.1 RF Digitizing

Due to many technological breakthroughs, it is now possible to digitize signals in the R.F. band and if this trend continues, it will be possible to place a digitizer in the antenna section of a receiver.

There are three main advantages to digitizing at the R.F. band. First, the noise figure of the receiver front-end can be kept to a minimum because only a few stages of amplification are necessary to provide the required gain to the digitizer. This in turn might increase the receiver sensitivity and it is the only method of obtaining information from the signal carrier frequency without adding excessive phase noise from the local oscillators. The information obtained in turn may describe some characteristics of the transmitter itself.

Finally, the expanding use of spread spectrum systems require wide bandwidth receiver front-ends in either the frequency hop or the direct sequence case. Either the spectrum spreading due to chip rate, or the frequency shift speed in frequency hop requires that the wide input bandwidth be instantaneous. With this in mind we can now look at the front-end complexity and at the signal processing required.

2.3.1.1 Receiver Front-End Complexity

Figure 2.3.1 (a) shows the basic block diagram of a receiver which uses R.F. digitization. Although the front-end section seems quite simple, the parameters describing the amplifier section which consists of several stages, are somewhat more difficult to obtain. Even though the RF technology is available for such a design, the limiting factor for this approach at this point might be the cost of implementation.

The two basic parameters which have an impact on the front-end design are:

i) The noise figure (NF)
ii) The spurious free dynamic range (SFDR)

The concepts associated with the noise figure of cascaded receiver components are well known while the concepts associated with optimizing cascaded receiver components for best spurious free dynamic range are less known.

As shown in Figure 2.3.2, (see Appendix H for explanation of Figure) these two parameters are inversely related, that is, if one is improved the other one deteriorates, therefore trade-off between sensitivity (probability of interception) and spurious free dynamic range (probability of detection) must be made.

From Figure 2.3.2 we can see that the front-end design requires these two parameters to be contained between the area bound by points <ABC>. Furthermore, if the bandwidth of the front-

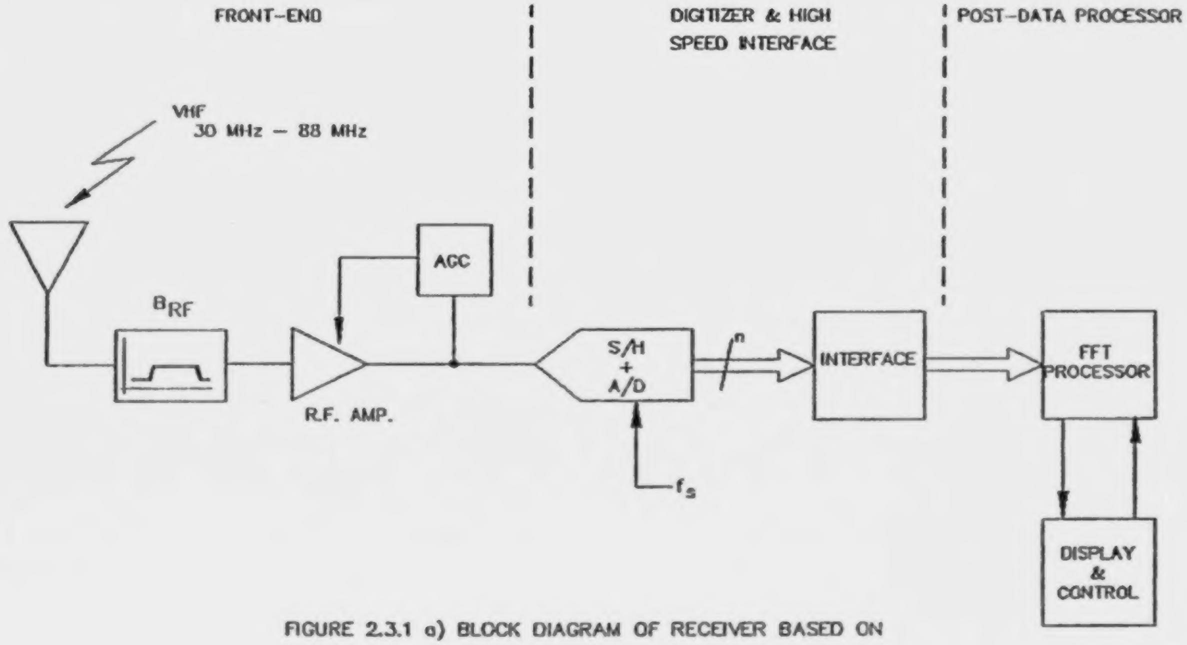
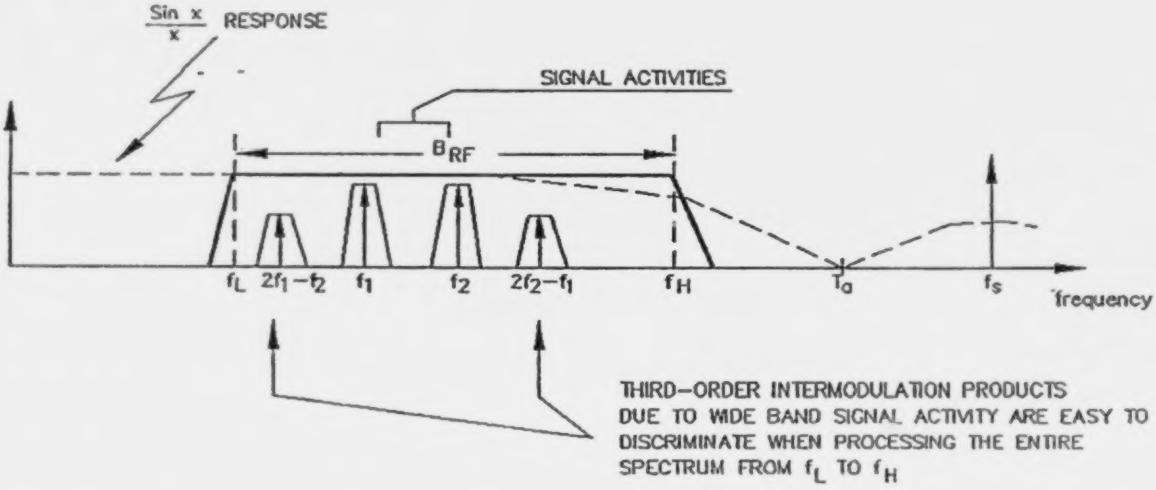


FIGURE 2.3.1 a) BLOCK DIAGRAM OF RECEIVER BASED ON R.F. DIGITIZATION



THIRD-ORDER INTERMODULATION PRODUCTS DUE TO WIDE BAND SIGNAL ACTIVITY ARE EASY TO DISCRIMINATE WHEN PROCESSING THE ENTIRE SPECTRUM FROM f_L TO f_H

FIGURE 2.3.1 b) R.F. SPECTRUM (VHF BAND)

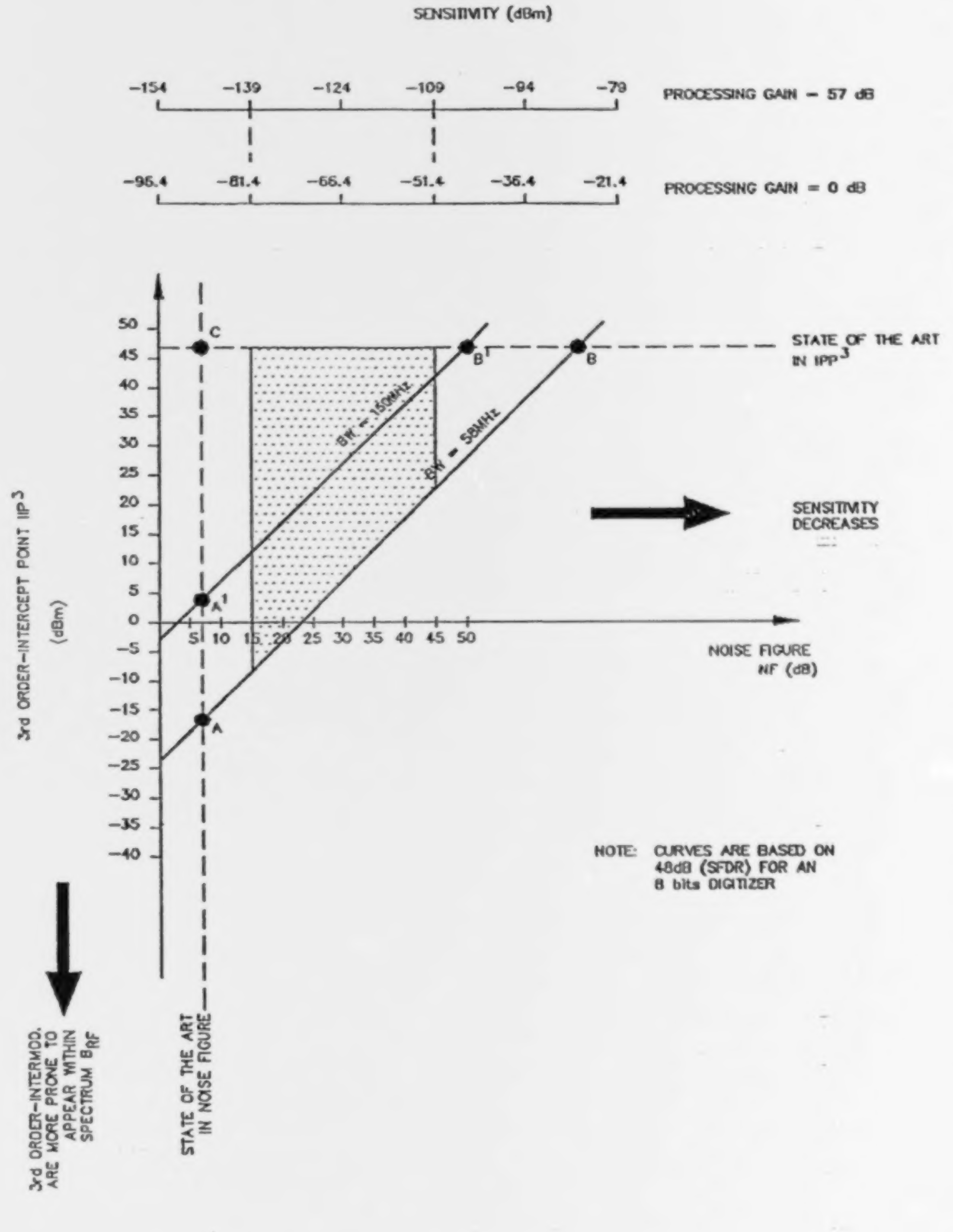


FIGURE 2.3.2 RELATIONSHIP OF NF AND IPP^3

FOR RF DIGITIZATION

end B_{RF} is increased, the area <A'B'C> becomes smaller and consequently the design becomes even more difficult to implement.

With R.F. digitization we require high sensitivity, (lowest N_F possible), large spurious free dynamic range (largest IIP^3 possible), and wide RF bandwidth. Trade-offs between these three parameters must be made. Figure 2.3.2 illustrates a possible design area (shaded area) which gives the optimum performance parameters for a receiver front-end designed to operate at 58 MHz and supplying a dynamic range compatible with an 8-bit digitizer.

2.3.1.2 Availability Of Digitizing Technology

Digitization at R.F. requires the fastest A/D available on the market today. Our survey indicates that the fastest A/D converters are the flash type. When using A/D converters, several parameters have to be met in order to properly digitize an R.F. signal. The parameters to be considered are the following:

a)	Number of bits	(n)
b)	Digitizing speed	(f_s)
c)	Aperture time	(T_a)
d)	Aperture uncertainty	(T_{aj})

The number of bits will determine the dynamic range achievable in the receiver design, therefore it is one of the most important parameters. However, the number of bits and digitizing speed are more or less inversely related due to the architecture of the flash converter itself. It is obvious then that R.F. digitization suffers from lack of bits available, and therefore dynamic range. Current technology can provide 8 bits at 300 MSPS (Sony CKA1176K) or 6 bits at 500 MSPS (Analog Devices AD9016). Tektronix also reportedly have a 500 MSPS 8 bit A/D ready for release.

Figure 2.3.3 illustrates a relationship between the number of bits and the dynamic range that can be achieved. The aperture time

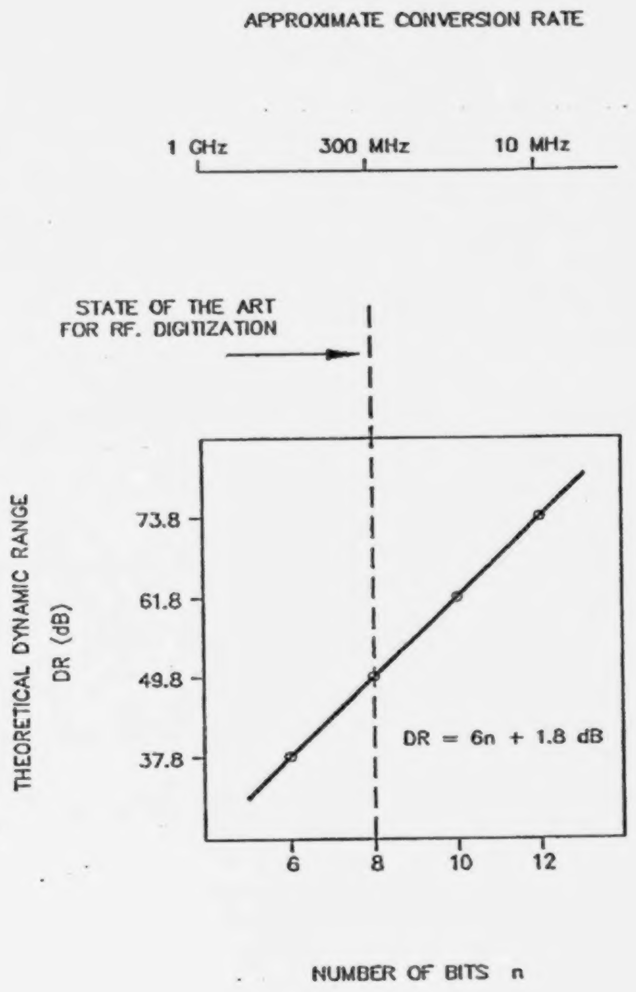


FIGURE 2.3.3 RELATIONSHIP OF DYNAMIC RANGE AND NUMBER OF BITS OF A DIGITIZER

T_a of an A/D will further reduce its dynamic range if not chosen carefully. The aperture time basically controls the (Sin X)/X response (see Figure 2.3.1 (b)). For good digitization in the band $B_{RF.}$ we try to keep the overall response as flat as possible by selecting an A/D or S/H amplifier with a very small Ta. Figure 2.3.4 illustrates the relationship of aperture time and the effective number of bits for an 8 and 6 bit digitizer (note the drop in effective dynamic range as the aperture time increases).

Sometimes the noise and distortion of flash A/D's suffer at very high conversion rates due to unequal propagation delays in the hundreds of comparators used to sense the input signal amplitude. With a large amplitude high frequency input signal, slew rate induced errors caused by these differential delays become serious, generating missing codes and causing linearity problems, which translate into poor noise performance and distortion. By adding a fast S/H ahead of the flash A/D, a sample of the input voltage can be held constant for the flash A/D, thus eliminating propagation delay errors due to slew rate. At high frequencies, improvements of 10 to 15 dB are achievable by adding a good S/H to a flash A/D.

Another important parameter which cannot be overlooked in R.F. digitization is the aperture uncertainty T_{aj} or in other words, the jitter in the aperture time.

The effect of this parameter on the digitization is to introduce noise, further reducing the available signal to noise ratio. Aperture uncertainty is given by the following equation:

$$T_{aj} = \frac{e_n}{\left.\frac{\partial e_s}{\partial t}\right|_{max.}} \qquad \text{eq. (18)}$$

where: e_n = error allowed in (LSB)

e_s = max. signal component frequency

BW = 88 MHz

f_{max} = 88 MHz

f_s = 176 MHz

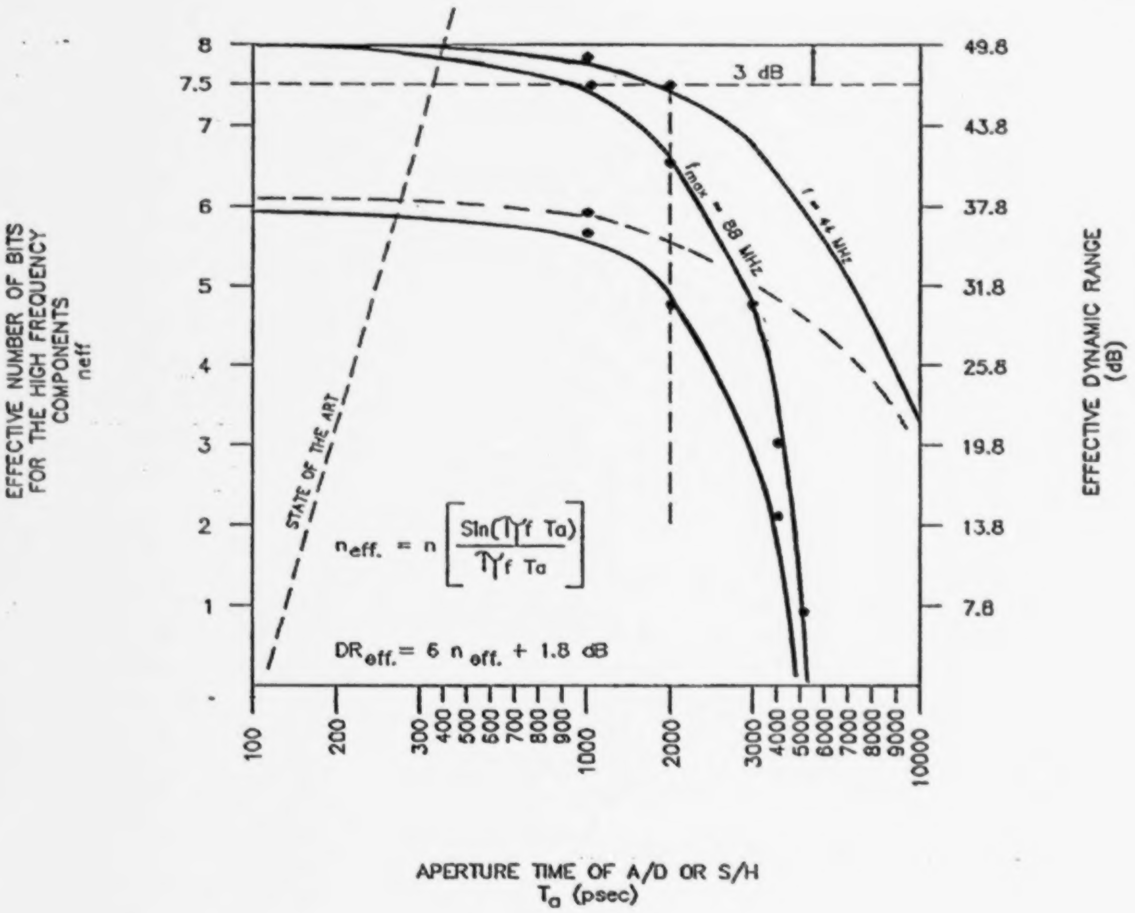


FIGURE 2.3.4 EFFECT OF THE SAMPLING RESPONSE ON THE HIGH FREQUENCIES COMPONENTS

Figure 2.3.5 illustrates the relationship of T_{ai} and the noise generated e_n for an 8 bit digitizer.

2.3.1.3 Post Processing Of Data

The final section of a receiver is the data processor sub-system. The trade-off that must be made here is the processing speed against the resolution (probability of detection). Figure 2.3.1 (b) illustrates the problem in extracting a signal when multiple signals are present within the R.F. band at the same instant in time.

The processor speed must be fast enough to track a frequency hopping signal having the order of 100 hops/sec. and it must have enough resolution to detect a signal of type (CW-OOK) which requires resolutions in the order of 100 Hz.

The type of processor used for spectral analysis is the Fast Fourier Transform (FFT) processor. This processor can be a superfast computer or a customized hardware processor. Figure 2.3.6 illustrates a speed versus resolution relationship for different types of FFT processors. Supposing we digitize at R.F. namely, the VHF band from 30 MHz to 88 MHz, in order to achieve a resolution of approximately 100 Hz, we need to compute a 524,288 point FFT. From Figure 2.3.6 we can see that there are some processors which can compute this FFT in a reasonable amount of time. What this means then, is that a receiver designed around such a processor can be classified as a "blinking" receiver.

Using an architecture similar to the one shown in Figure 2.3.7 it is possible to build a sophisticated post-processor with capabilities close to a "staring" type of receiver, therefore probabilities of interception close to 100% can be achieved. Furthermore, depending on the sophistication of the signal analysis sub-system, 100% probability of detection is also possible.

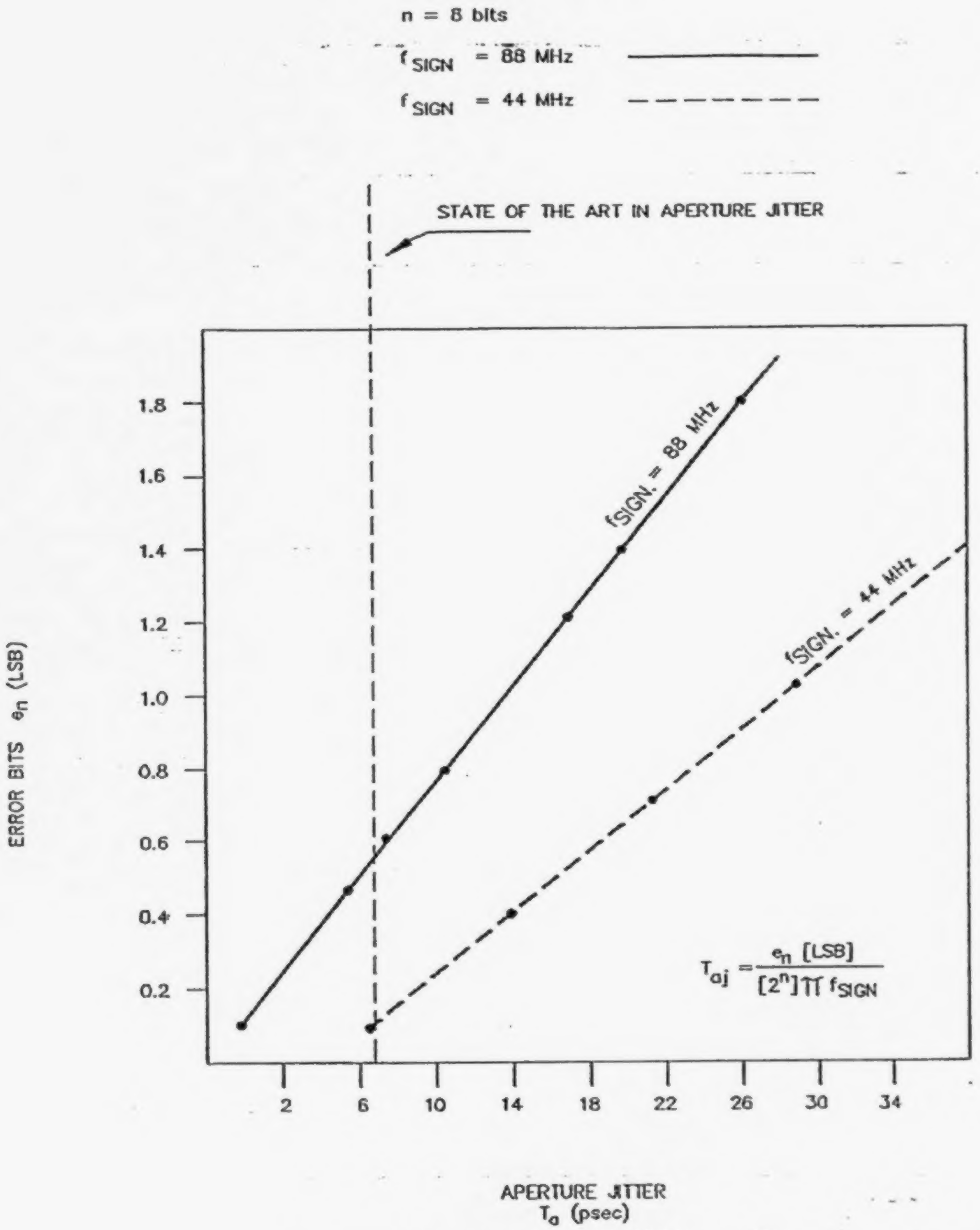


FIGURE 2.3.5 EFFECT OF APERTURE JITTER ON HIGH FREQUENCY COMPONENTS

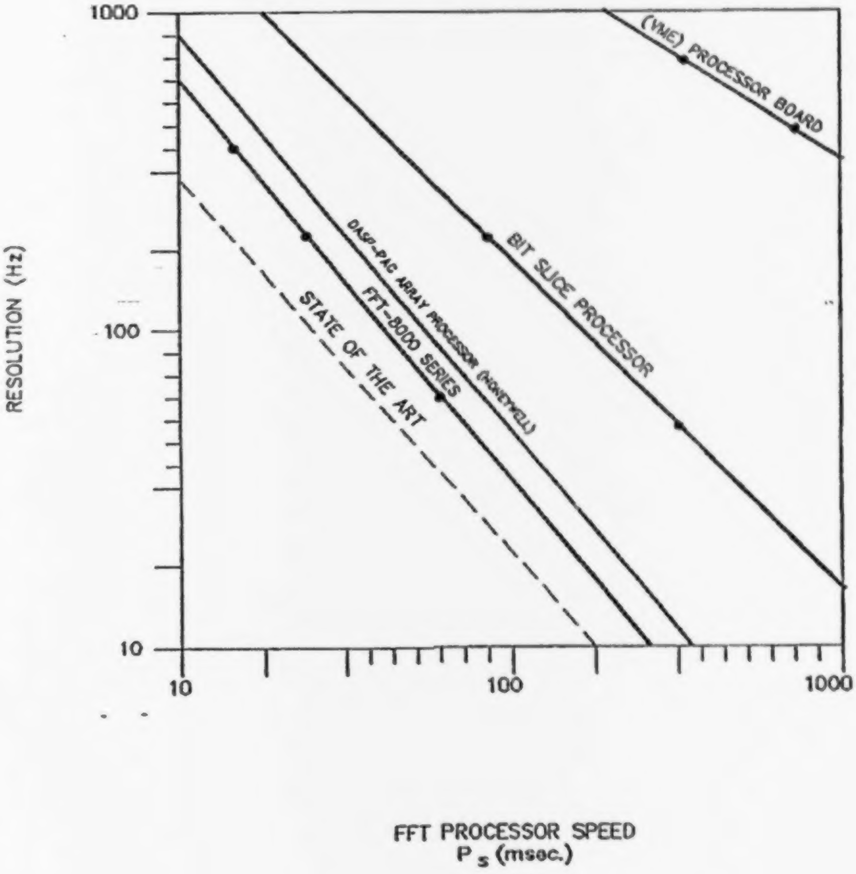
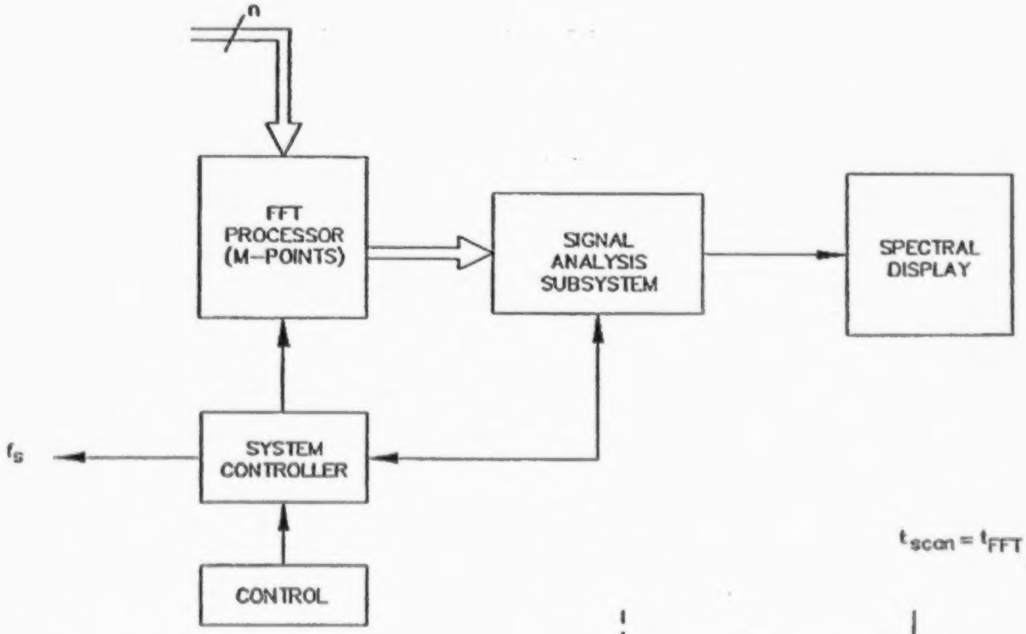
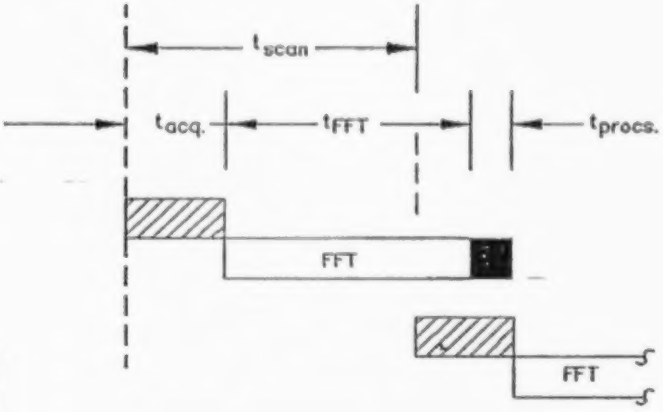


FIGURE 2.3.6 FFT PROCESSOR SPEED VS. RESOLUTION



$t_{scan} = t_{FFT} + t_{procs.}$



Resolution based on a
Bandwidth BW=58MHz

RESOLUTION (HZ)	$t_{scan.}$ (msec.)
14000	0.238
7080	0.476
3540	0.952
1770	1.904
885	3.808
442	7.616
221	15.23
110	30.4
55	60.9

FIGURE 2.3.7 POST–PROCESSOR ARCHITECTURE FOR RECEIVER USING R.F. DIGITIZATION

2.3.1.4 Conclusion

From this basic analysis we can conclude the following. With current state-of-the art technology we can digitize an R.F. signal at least on the VHF band with sensitivities ranging from -139 dBm to -109 dBm (Figure 2.3.2). The best signal to noise ratio achievable with careful design is 48 dB (8-bit digitizer) (Figures 2.3.2, 2.3.4 and 2.3.5).

And last, the resolution available is dependent on the FFT processor selected. Furthermore, from Section 2.3.1.3, a surveillance receiver with impressive characteristics can be implemented when digitization is done at RF. The only drawback here is cost.

2.3.2 I.F. Digitization

From the previous section we saw that digitization at R.F. was lacking dynamic range due to the current technology of A/D converters. In this section we are looking at digitization using a new approach, that is, harmonic sampling. With this method we can use a slower speed higher resolution A/D to digitally downconvert the baseband located at an I.F. frequency without loss of information.

There are other advantages of using harmonic sampling downconversion at an I.F. frequency, namely the use of quadrature programmable digital filters. With digital filters as we shall see in Section 2.3.2.3, the resolution bandwidth B_{res} can be totally programmable. Hence, the performance of the receiver in terms of resolution and scan rate can be controlled by a processor to suit different modes of operation.

Also, the post processor subsystem operates on less stringent parameters (same resolution for less points of the FFT). This in turn translates into easier implementation and lower costs.

2.3.2.1 Receiver Front-End Complexity

Figure 2.3.8 (a) illustrates a basic block diagram of a receiver which uses harmonic sampling at an I.F. frequency. Following a similar analysis as in Section 2.3.1.1, we see that the front-end design is more complicated in terms of components, therefore we would expect the noise figure to be higher in this case. Basing the analysis on a 12-bit digitizer, we can see from Figure 2.3.9 that indeed this is the case. The parameter design area bounded by points <ABC> decreased in size, thereby complicating the selection of devices and components for the front-end design. Since the state-of-the-art limits are not exceeded with the current technology, we can achieve a good front-end design and the only drawback is the cost of implementation.

2.3.2.2 Availability Of Digitizing Technology

Unlike the digitization at R.F., harmonic sampling uses medium speed A/D's. A survey of the current technology indicates that medium speed A/D's are also of the flash type.

Following the same description as in Section 2.3.1.2, the following parameters have to be chosen properly in order to digitize an I.F. band using the harmonic sampling method.

a) Number of bits
b) Digitizing speed
c) Aperture time
d) Aperture uncertainty

The number of bits will again determine the signal to noise ratio achievable in the receiver design, therefore it is still the most important parameter. Figure 2.3.10 illustrates the relationship between the number of bits and the dynamic range that can be achieved. Equations 19 and 20 control the selection of the sampling speed of the A/D Converter.

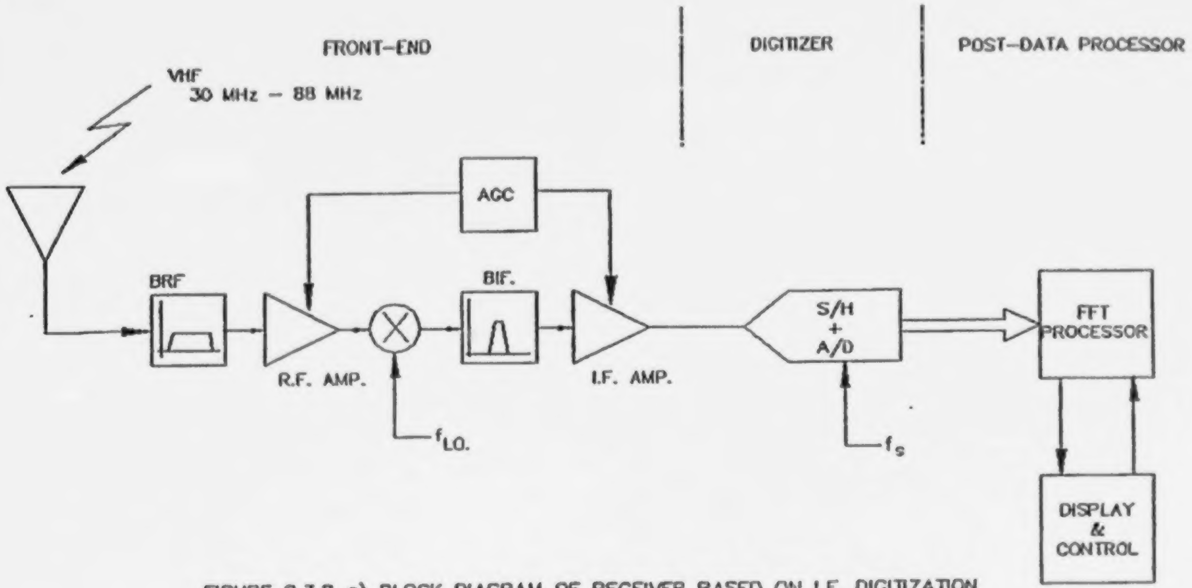


FIGURE 2.3.8 a) BLOCK DIAGRAM OF RECEIVER BASED ON I.F. DIGITIZATION

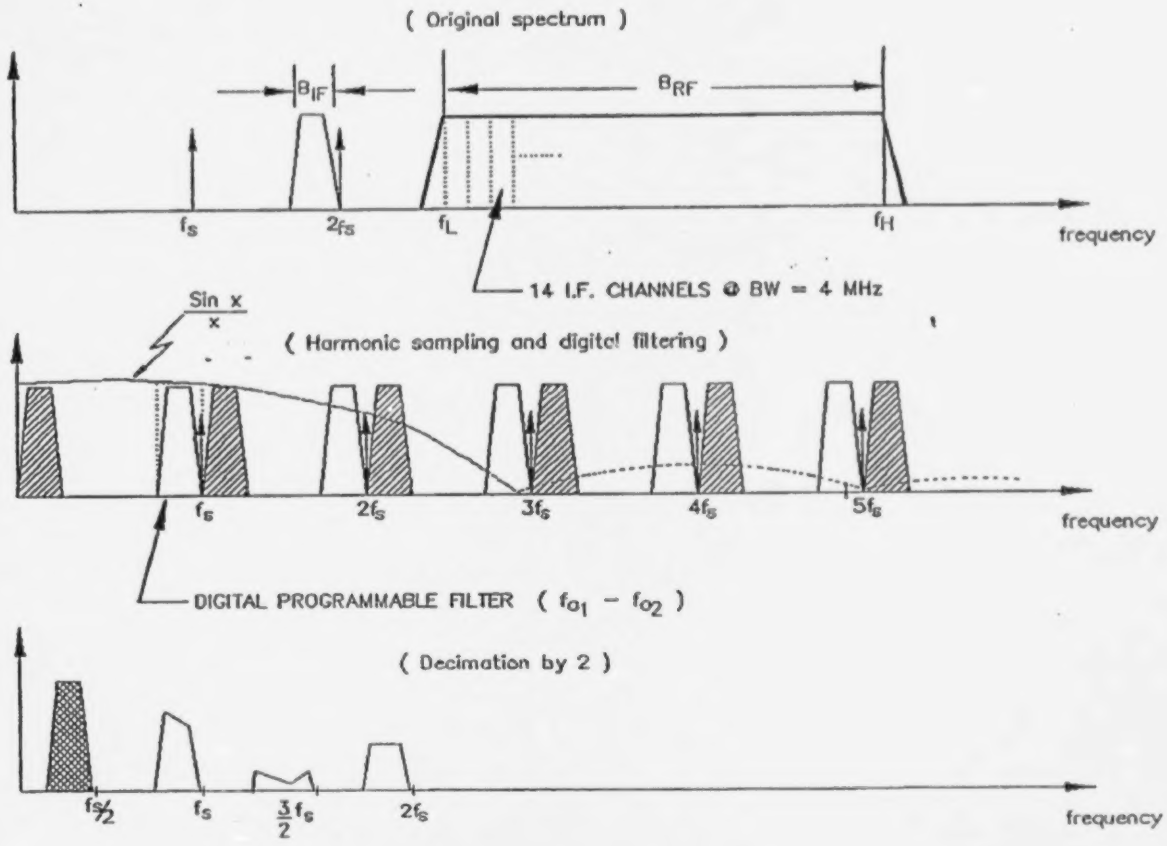


FIGURE 2.3.8 b) I.F. SPECTRUM WITH "HARMONIC SAMPLING"

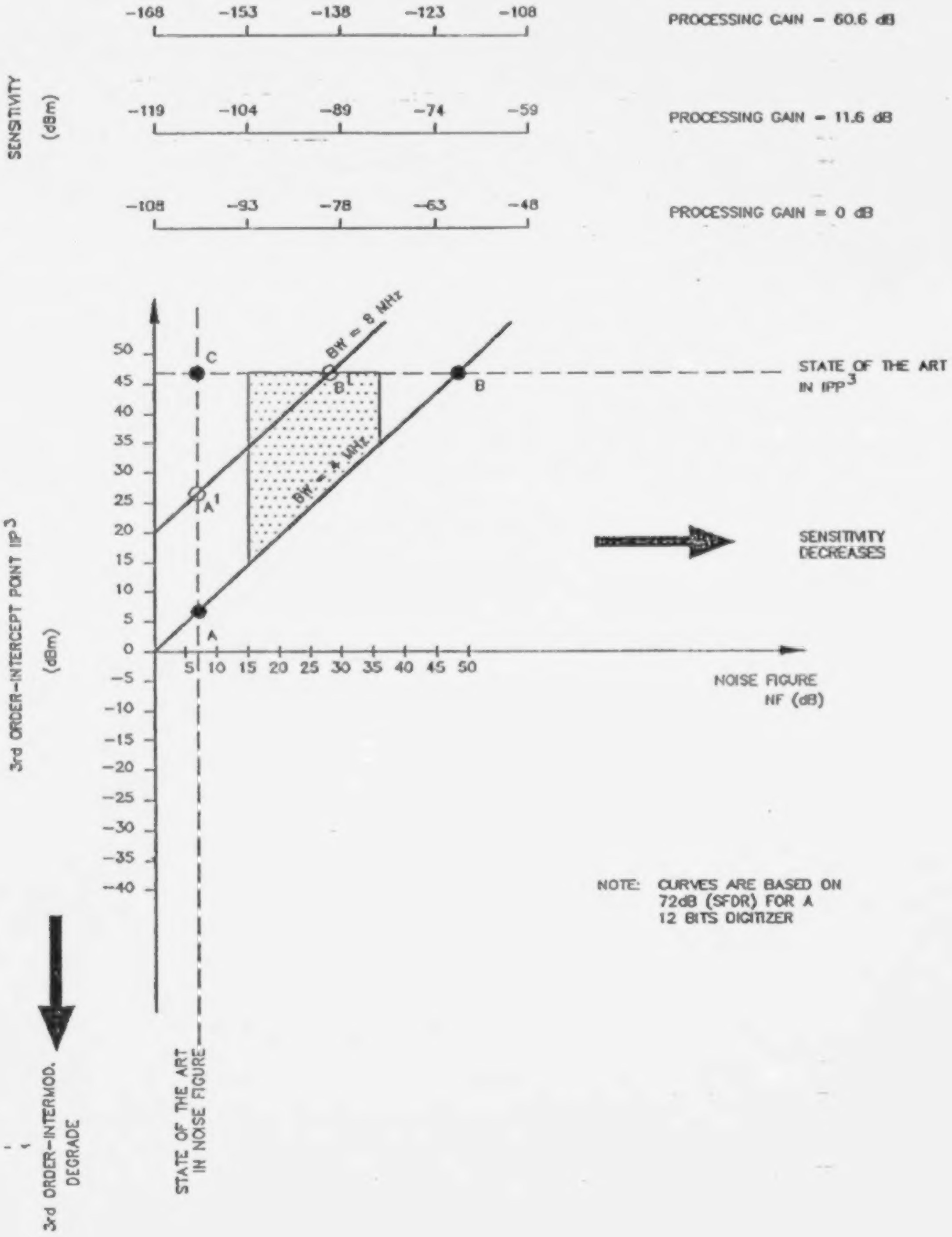


FIGURE 2.3.9 RELATIONSHIP OF NF AND IPP^3 FOR I.F. DIGITIZATION

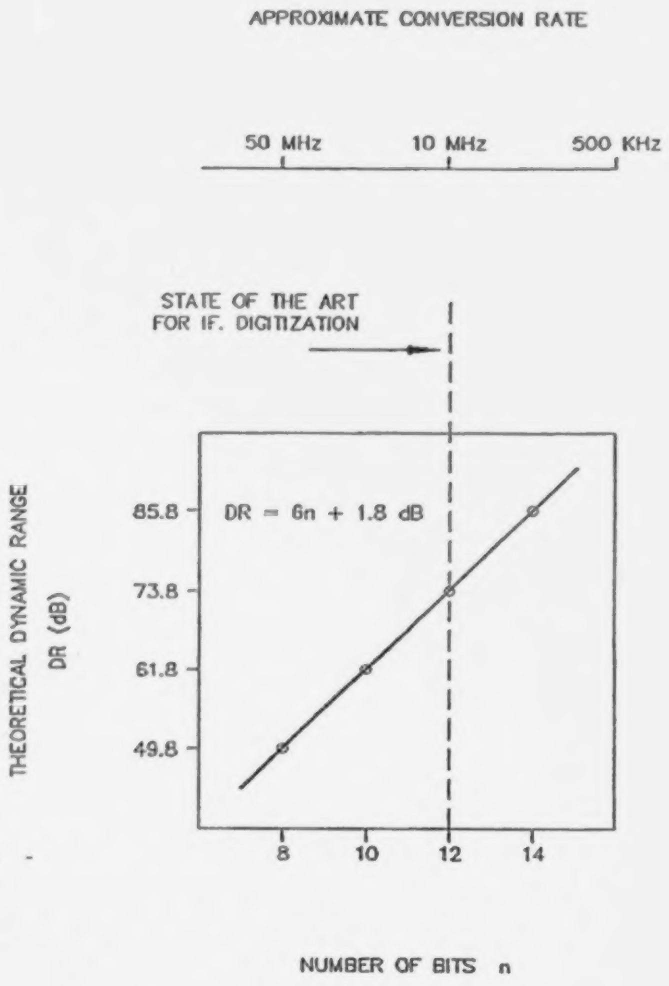


FIGURE 2.3.10 RELATIONSHIP OF DYNAMIC RANGE AND NUMBER OF BITS

$$fs = \frac{fHIF}{K} \qquad \text{eq. (19)}$$

$$\text{and} \quad fs \geqslant 2B_{IF} \qquad \text{eq. (20)}$$

where: f_s = sampling frequency
fH_{IF} = IF frequency + BIF/2
K = integer number
B = bandwidth of IF frequency

For K > 0, the band-pass signal is under sampled with respect to fH_{IF} but not with respect to B_{IF} and therefore no information is lost.

The aperture time of the A/D again plays an important role in selecting the right converter and/or a sample and hold amplifier. Figure 2.3.11 graphically illustrates the effective number of bits for an 8, 10 and 12 bit digitizer.

The next parameter that we shall analyze is the aperture uncertainty. Using equation (18), we can generate this result graphically in Figure 2.3.12. Again, if this parameter is not chosen carefully, degradation in dynamic range at the upper frequencies becomes a problem.

2.3.2.3 Post Processing Of Data

Looking back at Figure 2.3.8(a), the post processing of I.F. information seems more complicated than when R.F. digitization is performed. This is not the case however, because processing is performed on smaller sets of data at a rate controlled by the Receiver System Controller which can be mode selected depending on the surveillance receiver design. From this we can see that stringent parameters such as the 524,288 FFT processing speed, acquisition time and fast data memory buffer are relieved when digitization is performed at the I.F. frequency using harmonic sampling.

$BW = 4 \text{ MHz}$

$f_{IF} = 21.4 \text{ MHz}$

$f_{max} = f_{IF} + BW_{IF} /2$

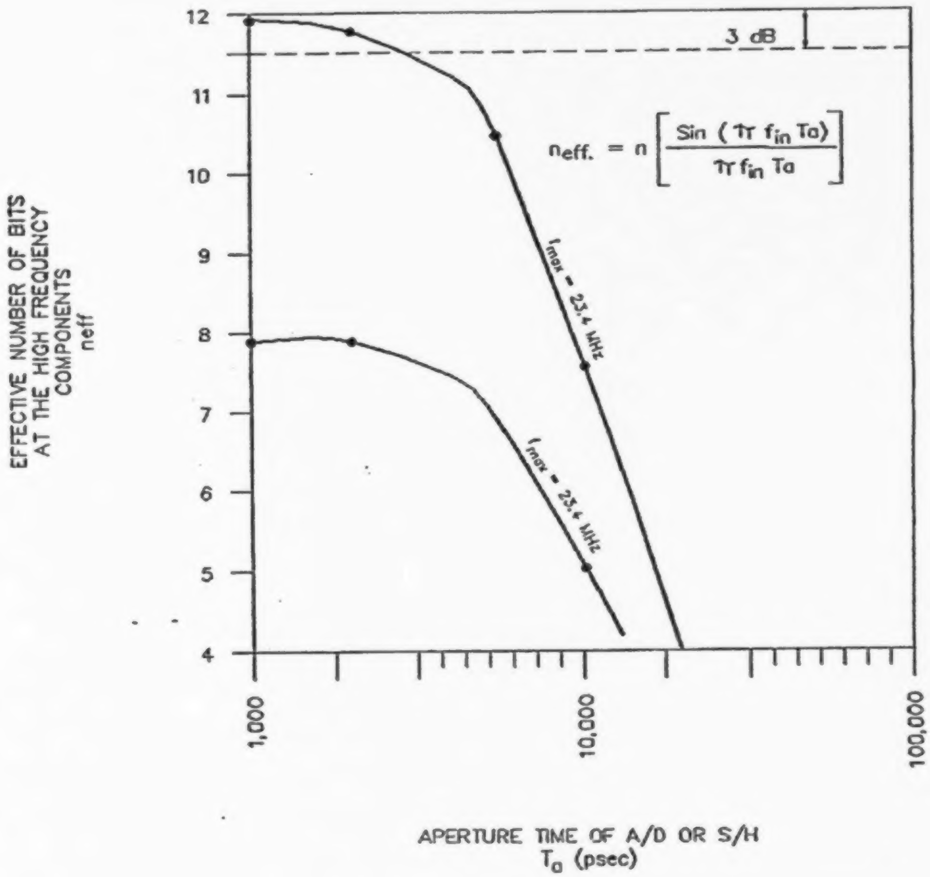


FIGURE 2.3.11 EFFECT OF THE SAMPLING RESPONSE ON THE HIGH FREQUENCY COMPONENTS

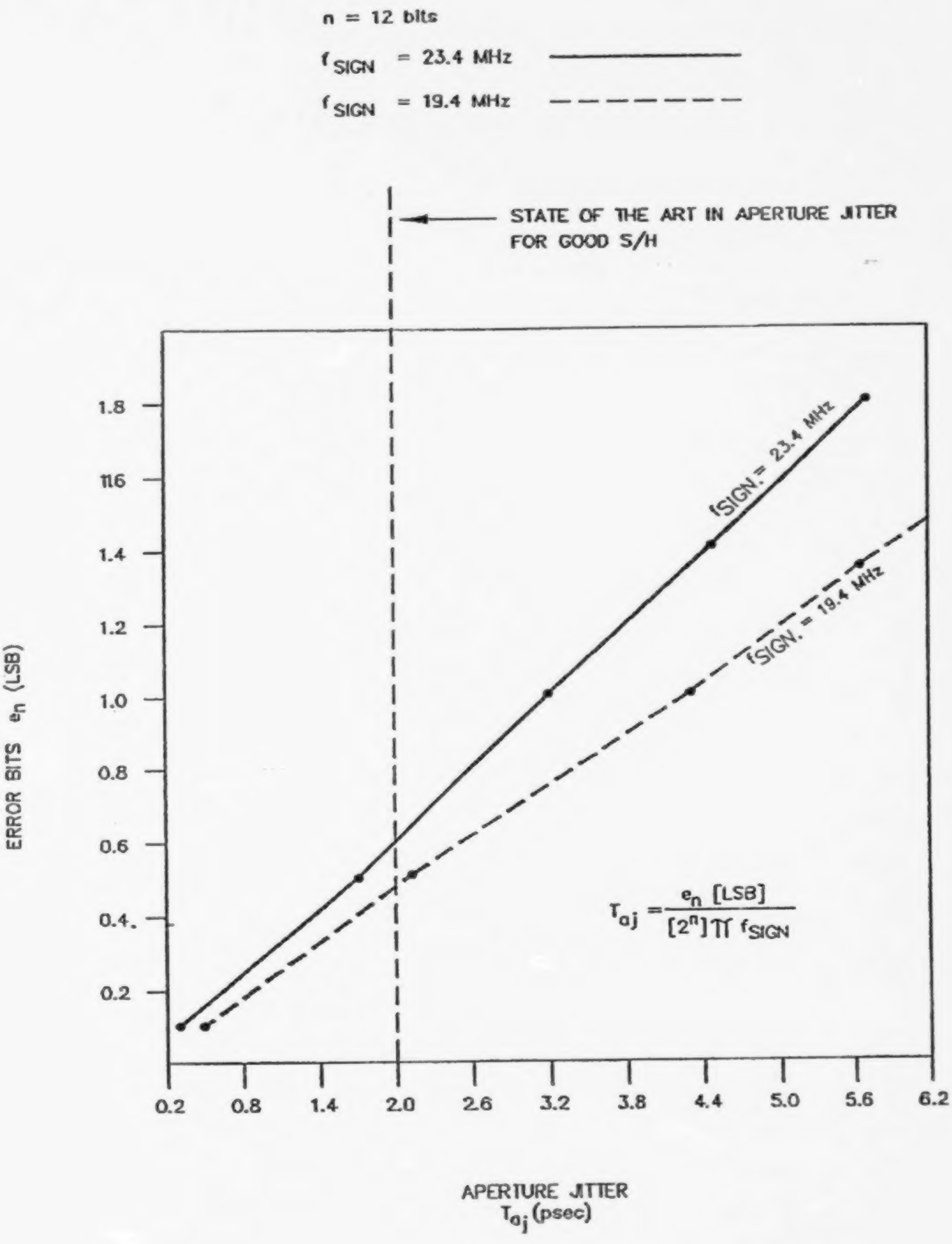


FIGURE 2.3.12 EFFECT OF APERTURE JITTER ON THE HIGH FREQUENCY COMPONENTS

Figure 2.3.8(b) illustrates how the R.F. band is broken down into 14 sub-bands and how each is translated to the IF frequency with a 4 MHz bandwidth. The 4 MHz band in turn is translated to fo_1-fo_2 by the digital filter (due to harmonic sampling) which can be programmed for a second pass to 20 sub-sub-bands each of which has a bandwidth of 200 KHz. If we use a 4096 point FFT we can achieve a resolution of approximately 48 Hz. From Figure 2.3.6, a 4K point FFT takes only 0.238 msec with an ECL based processor; therefore if we repeat this process over the entire B_{RF} band, we can intercept virtually any signal activity.

A surveillance receiver designed around such a concept would be classified as a scanning type. Depending on the sophistication of the interception algorithm and the scanning bandwidth, the receiver could have a 100% probability of detection provided the signal activity on any I.F. band last longer than the total scanning time.

Figure 2.3.13 illustrates an oversimplified block diagram for a post processor. Using state-of-the-art technology with an optimized design, it is possible to implement a receiver which has parameters similar to the one described in Figure 2.3.13.

2.3.2.4 Conclusion

In this basic analysis we can conclude that with today's state-of-the-art we can digitize an I.F. signal using harmonic sampling with possible sensitivities ranging from -104 dBm to -74 dbm with a single pass of FFT. Sensitivities of -153 dBm to -123 dBm are possible with a double pass of FFT (see Figure 2.3.9). The best signal to noise ratio achievable with careful design is 72 dB (12-bit digitizer). (See Figures 2.3.10, 2.3.11 and 2.3.12 for parameters required by the A/D). From Section 2.3.2 we can therefore conclude that a scanning type of receiver can be implemented having the following characteristics:

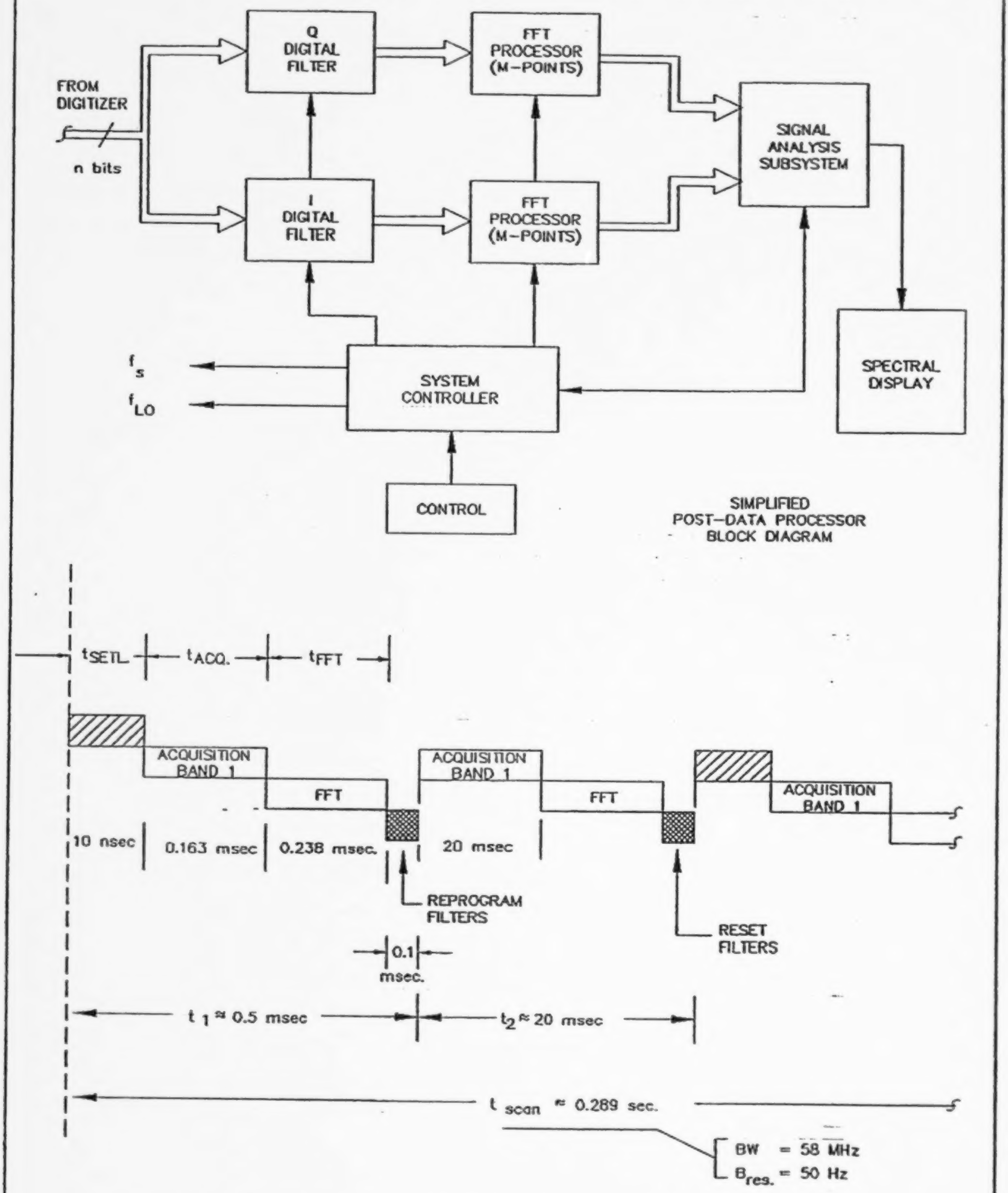


FIGURE 2.3.13 POST–PROCESSOR ARCHITECTURE FOR RECEIVER USING I.F. DIGITAIZATION

BW = 58 MHz

B_{res} = 50 Hz

Total Scan Speed = 0.289 sec

Signal to Noise Ratio = 72 dB

2.3.3 Baseband Digitization

Digitization at baseband makes things a little easier as far as the A/D converter selection is concerned. A survey of the technology indicates that many manufacturers can supply A/D's with 16 bits of quantization and with speeds appropriate for baseband applications.

The main advantage of digitizing at baseband is to obtain a very large dynamic range (note: a 16-bit A/D can provide up to 96 dB of dynamic range) with the result of increasing the receiver sensitivity.

Another advantage is the post processor resolution bandwidth, since the second IF is demodulated to baseband (180 KHz for FM broadband) then with a single pass FFT (4096 points) we can obtain resolutions of approximately 40 Hz. One major drawback of digitization at baseband is the settling time of the local oscillator frequency synthesizers. If the receiver is used as a scanning type of surveillance receiver, then the combined settling time plus the acquisition and processing times must be short in order to have a good probability of interception.

2.3.3.1 Receiver Front-End Complexity

Figure 2.3.14(a) illustrates a basic block diagram of a receiver which uses baseband digitization. Following a similar analysis as in the previous sections, we see that the front-end involves a number of components, therefore we would expect the parameters describing this section to be stringent, from a designer point of view.

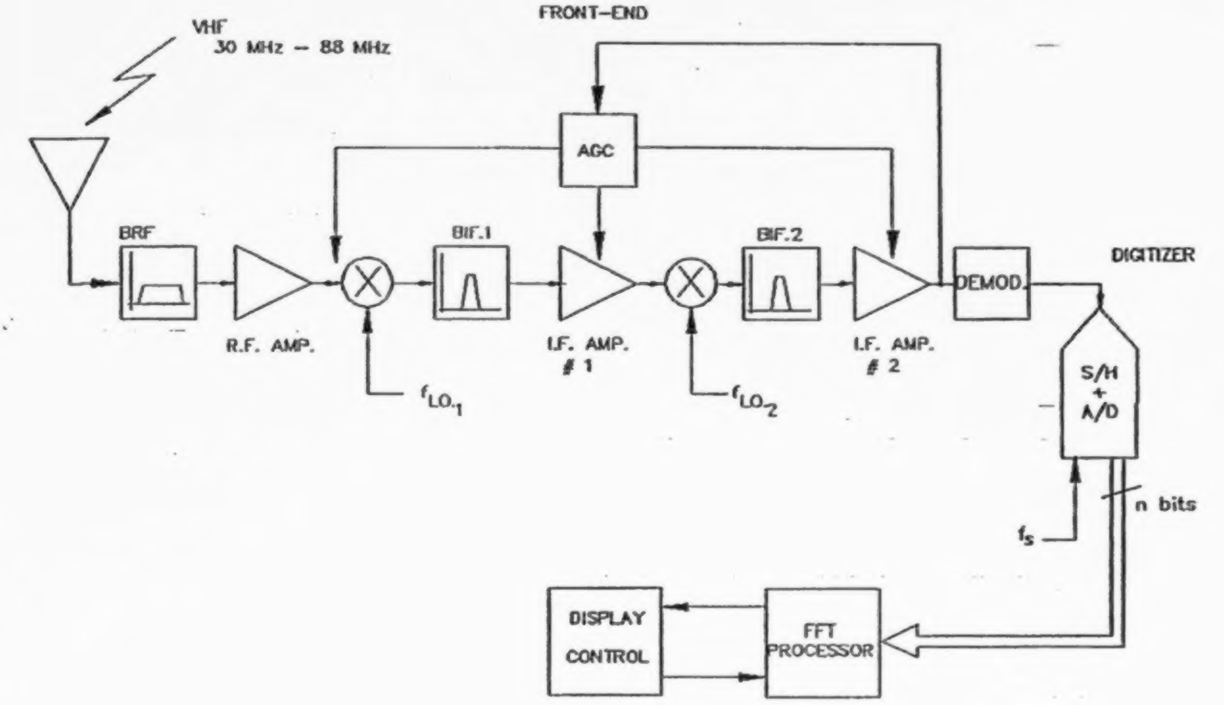


FIGURE 2.3.14 a) BLOCK DIAGRAM OF RECEIVER BASED ON BASEBAND DIGITIZATION

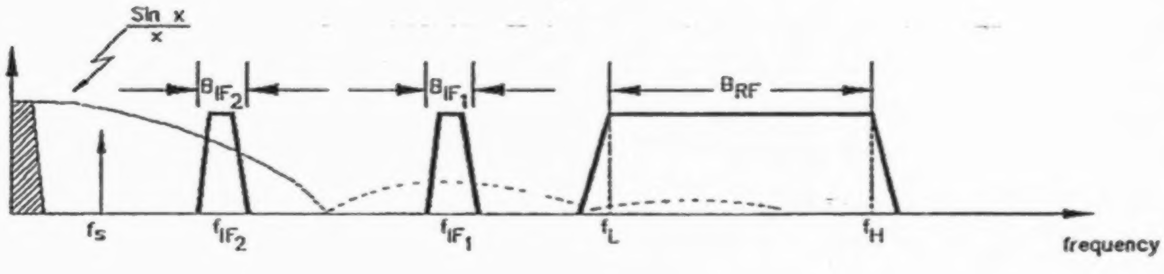


FIGURE 2.3.14 b) BASEBAND SPECTRUM

Figure 2.3.15 shows that this is indeed the case (analysis was based on a 16 bit digitizer). In this plot the parameter design area bounded by points <ABC> is even smaller compared to the previous types of digitization with the result of complicating the front-end design even further.

Again, state-of-the-art limits are not exceeded thereby making the design possible presumably at an elevated cost as compared to previous methods of digitization.

2.3.3.2 Availability Of Digitizing Technology

Digitization at baseband uses the highest resolution A/D converters available on the market today. Following the same description as in the previous sections, we can show graphically the limits of the parameters needed in order to digitize at baseband. Figures 2.3.16, 2.3.17 and 2.3.18 data is based on a baseband bandwidth of 180 KHz with sampling rates f_s = 360 KHz. As we can see, any of these parameters are easily achievable with current technology. Note however, that a good sample and hold amplifier must be inserted in front of any A/D in order to minimize the aperture time uncertainty parameter.

2.3.3.3 Post Processing Of Data

Figure 2.3.14 illustrates the quadrature complex post processor needed in a baseband digitization system. Here the digital filters are the lowpass type, since the information is already demodulated. A 4K FFT processor will give a resolution of approximately 40 Hz on each channel during a single pass, therefore the filter does not need to be reprogrammed by the system controller. However, if finer resolutions are needed, this concept allows for total reprogramability of the various digital components.

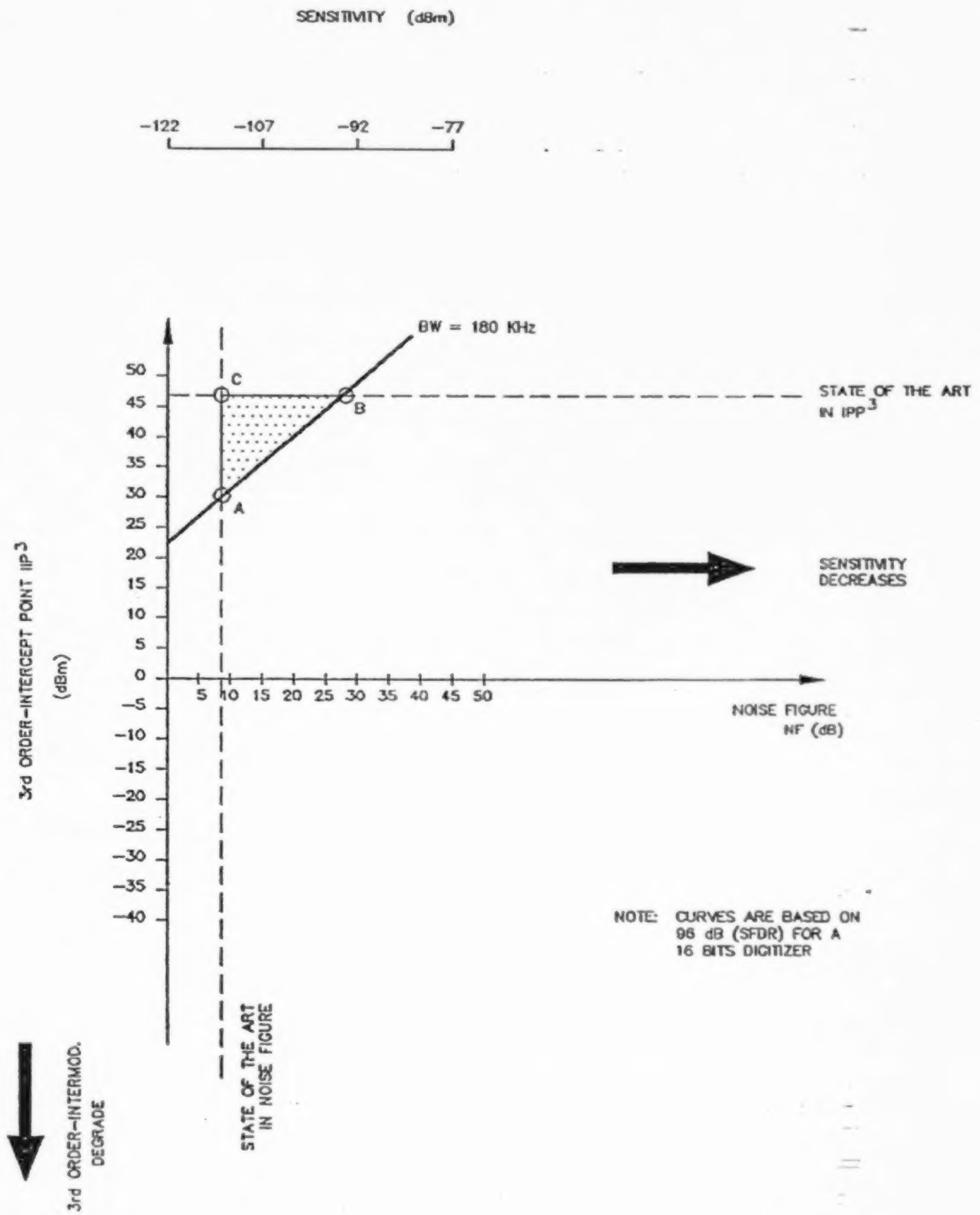


FIGURE 2.3.15 RELATIONSHIP OF NF AND IIP^3 FOR BASEBAND DIGITIZATION

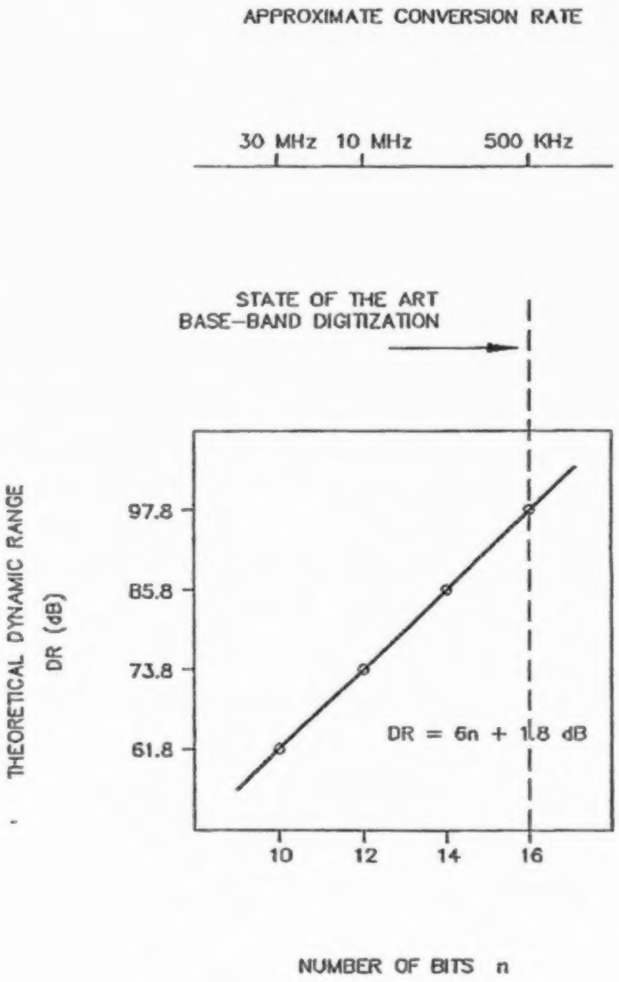


FIGURE 2.3.16 RELATIONSHIP OF DYNAMIC RANGE AND NUMBER OF BITS

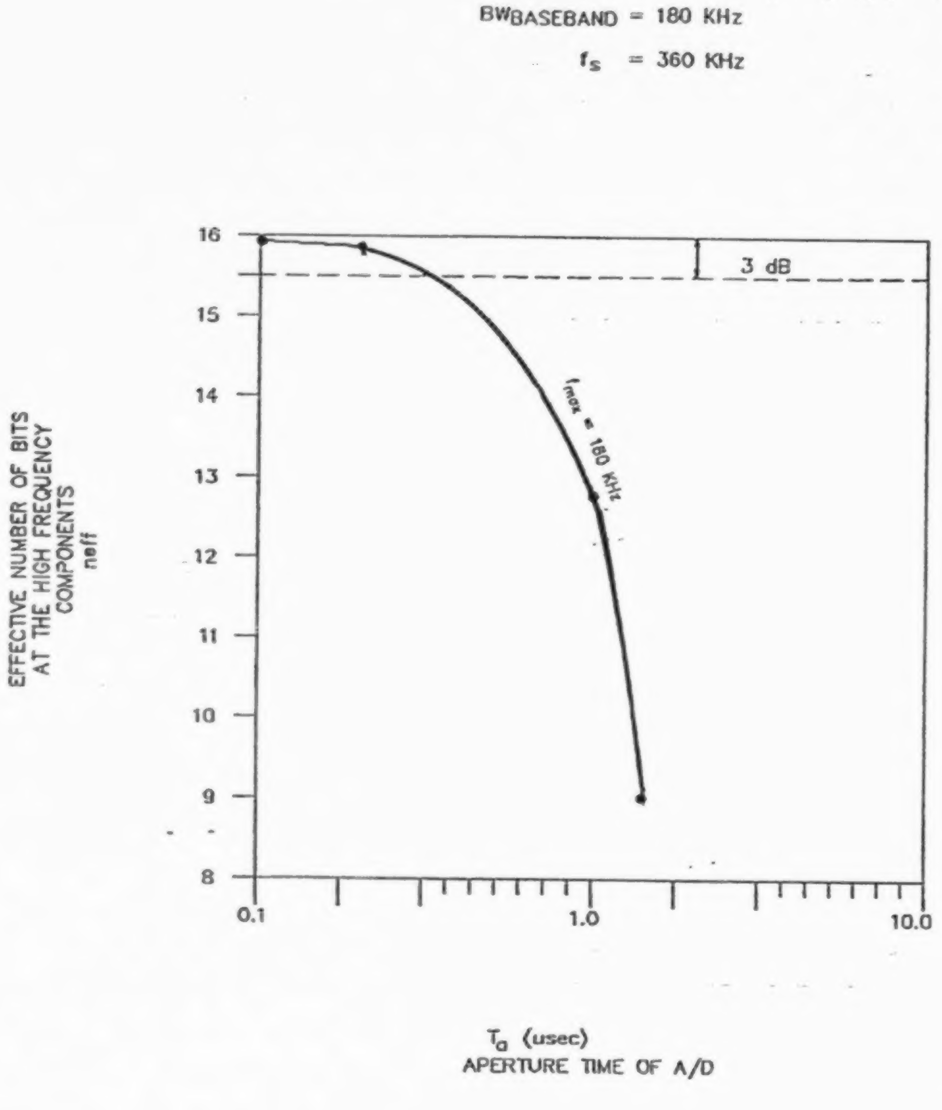


FIGURE 2.3.17 EFFECT OF THE SAMPLING RESPONSE ON THE HIGH FREQUENCY COMPONENTS

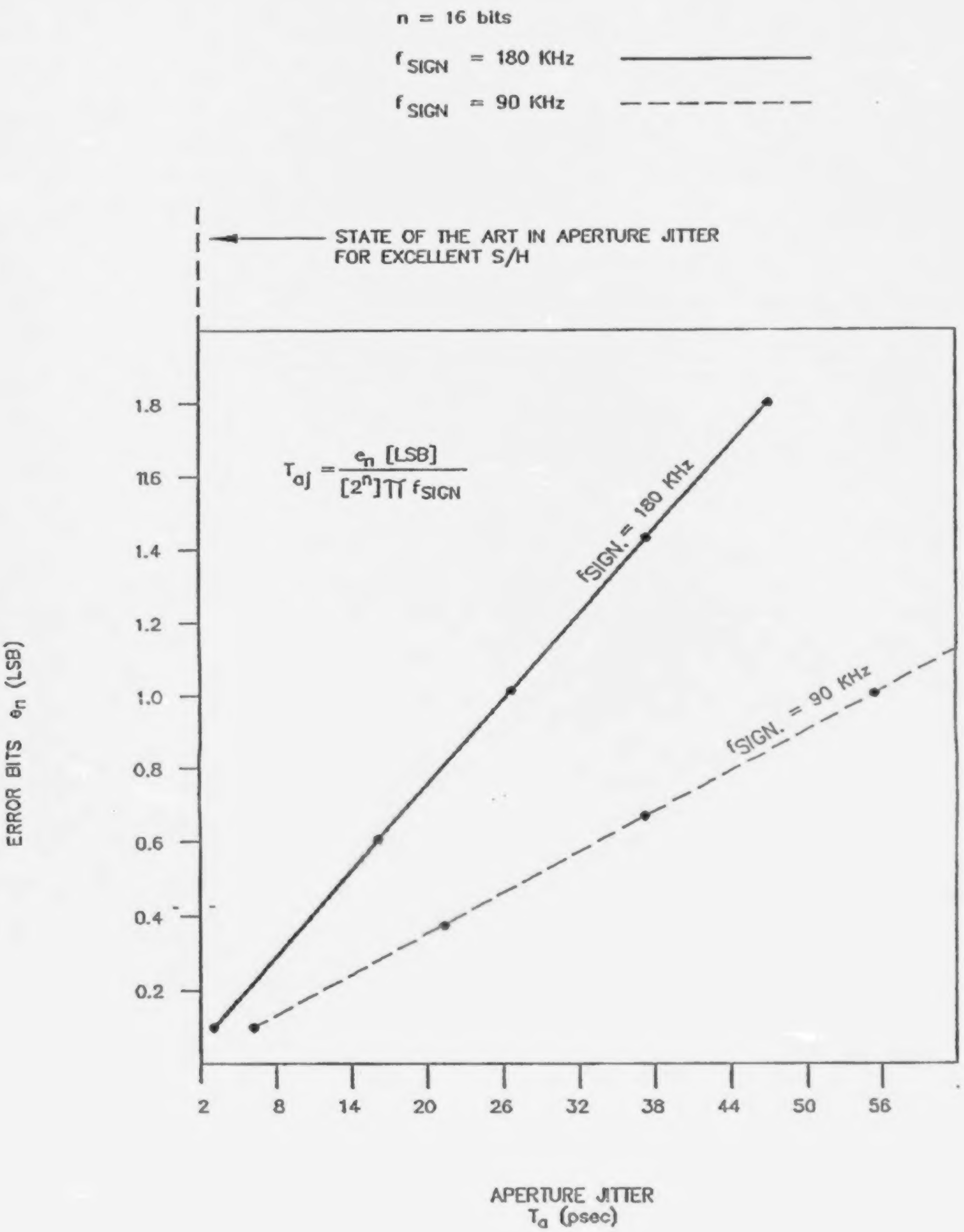


FIGURE 2.3.18 EFFECT OF APERTURE JITTER ON THE HIGH FREQUENCY COMPONENTS

The most critical parts in this realization are the frequency synthesizer for both local oscillators fLO_1, and fLO_2. In order to achieve a fast scanning speed, these synthesizers must settle very quickly to the final fLO.

A surveillance receiver designed around this concept can be classified as a scanning type, and depending on the sophistication of the interception algorithm and the scanning bandwidth, the receiver could have a 100% probability of intercept on a small bandwidth.

Finally, Figure 2.3.19 illustrates an oversimplified block diagram for a post processor using state-of-the-art technology to achieve a high dynamic range using baseband digitization.

2.3.3.4 Conclusion

Digitization at baseband involves a sophisticated analog front-end requiring stringent parameters in order to provide the digitizer with a dynamic range of approximately 96 dB and a spurious free spectrum. Sensitivities achievable with state-of-the-art design and components are in the order of -107 dBm to -92 dBm (without processing gain).

The baseband frequency resolution can be in the order of 40 Hz for a single pass or even finer for a double pass FFT. This will depend on the level of sophistication of the receiver designed around this concept.

A scanning type receiver can be implemented with the following characteristics:

BW = 58 MHz
B_{res} = 40 Hz
Total scan speed = 3.23 sec.
Signal to Noise Ratio = 96 dB

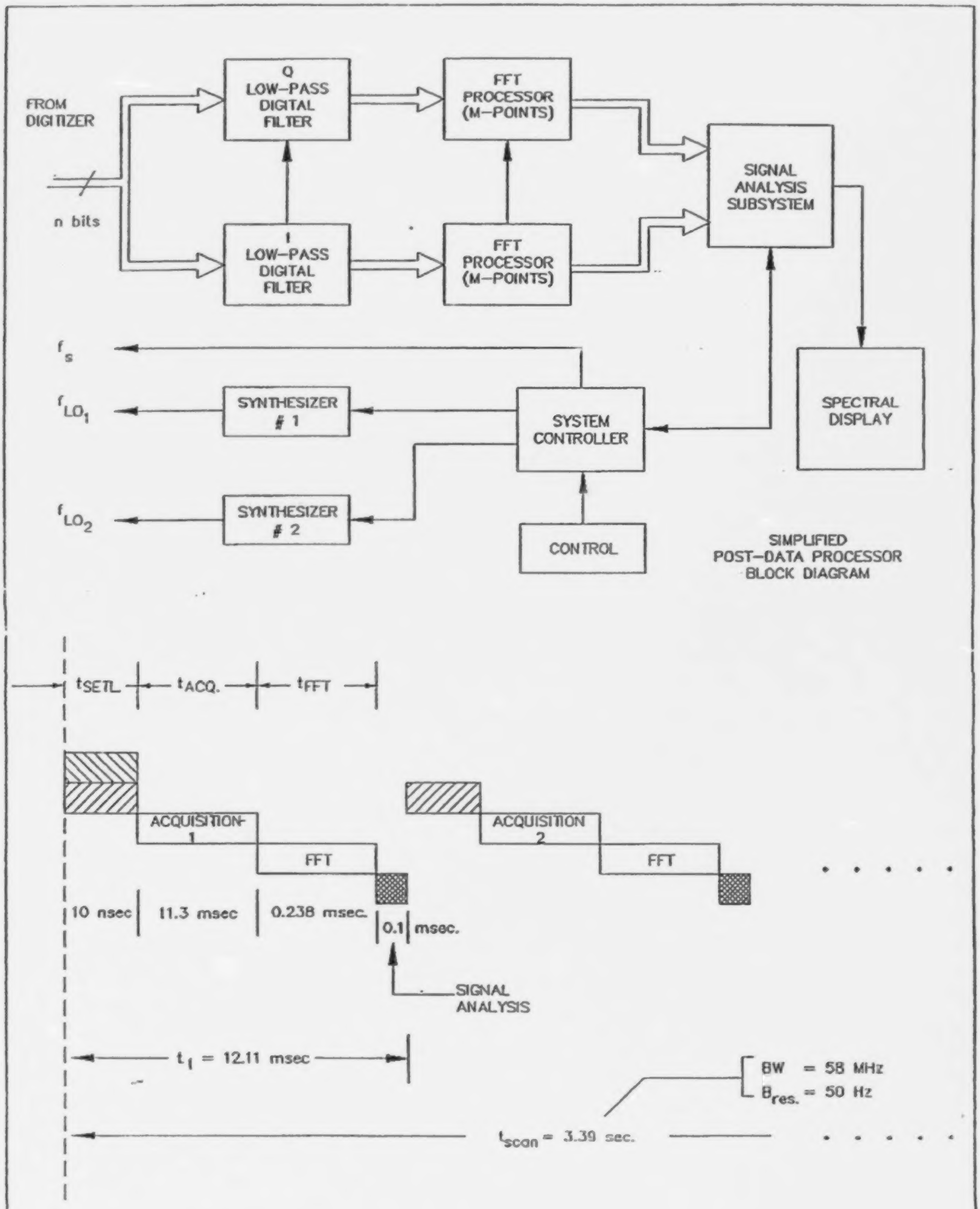


FIGURE 2.3.19 POST-PROCESSOR ARCHITECTURE FOR RECEIVER USING BASEBAND DIGITIZATION

2.3.4 Trade-Off Considerations

With current state-of-the-art technology, we conclude that digitization at the R.F. band (VHF), I.F. band and baseband are all feasible. However, trade-offs must be made in terms of cost, dynamic range, sensitivity, resolution, processing time, flexibility of the design and overall receiver complexity. Table 2.3.1 illustrates the parameters derived from this study to make these trade-off considerations.

The recommendation of where digitization should be performed on a surveillance type of receiver have been based on conclusions derived from Table 2.3.1. As we can see from this table, cost and dynamic range seem to be the two parameters which differ the most from one stage of digitization to another.

I.F. digitization can offer a design with relatively low cost when compared to the other two methods of digitization. Therefore, we can rule out R.F. digitization because of poor dynamic range and high cost unless information about the carrier frequency is required, which would lead us to have no choice but to digitize at R.F. Otherwise, a decision between I.F. and baseband digitization must be made.

If we analyze the complexity of design and also the difficulty of achieving 96 dB of dynamic range in the case of baseband, we can definitely say that I.F. digitization offers a more clear cut solution of design with a fairly reasonable dynamic range.

		R.F. DIGITIZATION	I.F. DIGITIZATION	BASEBAND DIGITIZATION
COST	ANALOG FRONT-END	FAIRLY LOW	HIGHER THAN R.F. DIGITIZ.	HIGH PARAMETERS ARE DIFFICULT TO ACHIEVE
	PROCESSOR	VERY HIGH	LOW DEPENDS ON DETECTION SUBSYSTEM	LOW DEPENDS ON DETECTION SUBSYSTEM
DYNAMIC RANGE		LOW 48 dB	GOOD 72 dB	EXELLENT 96 dB VERY DIFFICULT TO ACHIVE
SENSITIVITY		RANGING FROM: -139 dBm TO -109 dBm	RANGING FROM: -130 dBm TO -74 dBm	RANGING FROM: -107 dBm TO -92 dBm
RESOLUTION		APPROX. = 100 Hz ON BW = 58 MHz. 524,288 POINT FFT	APPROX. = 50 Hz ON BW = 4 MHz. 4096 POINTS FFT (DUAL PASS)	APPROX. = 40 Hz ON BV = 180 KHz 4096 POINTS FFT (SINGLE PASS)
PROCESSING TIME		APPROX. = 46 nsec. (BUT DEPENDS ON RESOLUTION)	APPROX. = .23 sec. -FULL SCAN OF 58 MHz -PROCESSING ON BW = 4MHz	APPROX. = 3.39 sec. -FULL SCAN OF 58 MHz -PROCESSING ON BV = 180 KHz
FLEXIBILITY OF DESIGN		ONLY RESOLUTION CAN BE CONTROLLED (USUALLY IS FIXED)	MICROPROCESSOR CAN CONTROL DIFFERENT MODES OF OPERATION	MICROPROCESSOR CAN CONTROL DIFFERENT MODES OF OPERATION
PHASE NOISE ADDED BY THE SYSTEM		VERY LOW	LOW	SUBSTANTIAL
DATA RATE		VERY HIGH	RELATIVELY LOW	LOW
OVER ALL COMPLEXITY OF DESIGN	ANALOG	VERY SIMPLE IMPLEMENTATION	SIMPLE IMPLEMENTATION	COMPLEX IMPLEMENTATION
	PROCESSOR	STRAIGHT FORWARD CONCEPT BUT EXPENSIVE	EASY IMPLEMENTATION MICROPROCESSOR PLUS DIGITAL SUBSYSTEM	EASY IMPLEMENTATION MICROPROCESSOR PLUS DIGITAL SUBSYSTEM

TABLE 2.3.1 COMPARISON OF TYPES OF DIGITIZATIONS

3.0 OVERALL SYSTEM CONSIDERATIONS

In this section we shall analyze parameter trade-offs in a receiver system. To begin, system operating conditions and performance requirements have to be determined.

3.1 Communication Receiver Signal Environment

Today's communication surveillance receivers are challenged by a dense, complex and constantly changing electronic signal environment. On the input side, the signal environment is growing denser while the threats are exhibiting multiple parameter agilities and low probability of intercept qualities. On the output side, the processors are demanding orders of magnitude increases in per pulse probability of intercept and complete parameter encoding of every detected signal. The net result is a set of receiver specifications exceeding current capabilities.

Meeting this challenge will require not only advanced receiver technologies but also new receiver architectures and utilization strategies.

3.2 The Need For A Receiver Architecture

Systems designed around a single receiver type will never achieve optimum performance due to the inherent limitations single receiver types have. They cannot be expected to perform the full span spectral surveillance (ie, high probability of intercept at one instant followed by high resolution analysis the next). Also they tend to become obsolete rather fast as technology keeps advancing.

What is needed then is a modular type of architecture which is flexible in terms of interfacing, programmability for different missions, expandable in width (frequency coverage) and depth (signal analysis resolution), and most importantly that the design will be able to follow the technology trend.

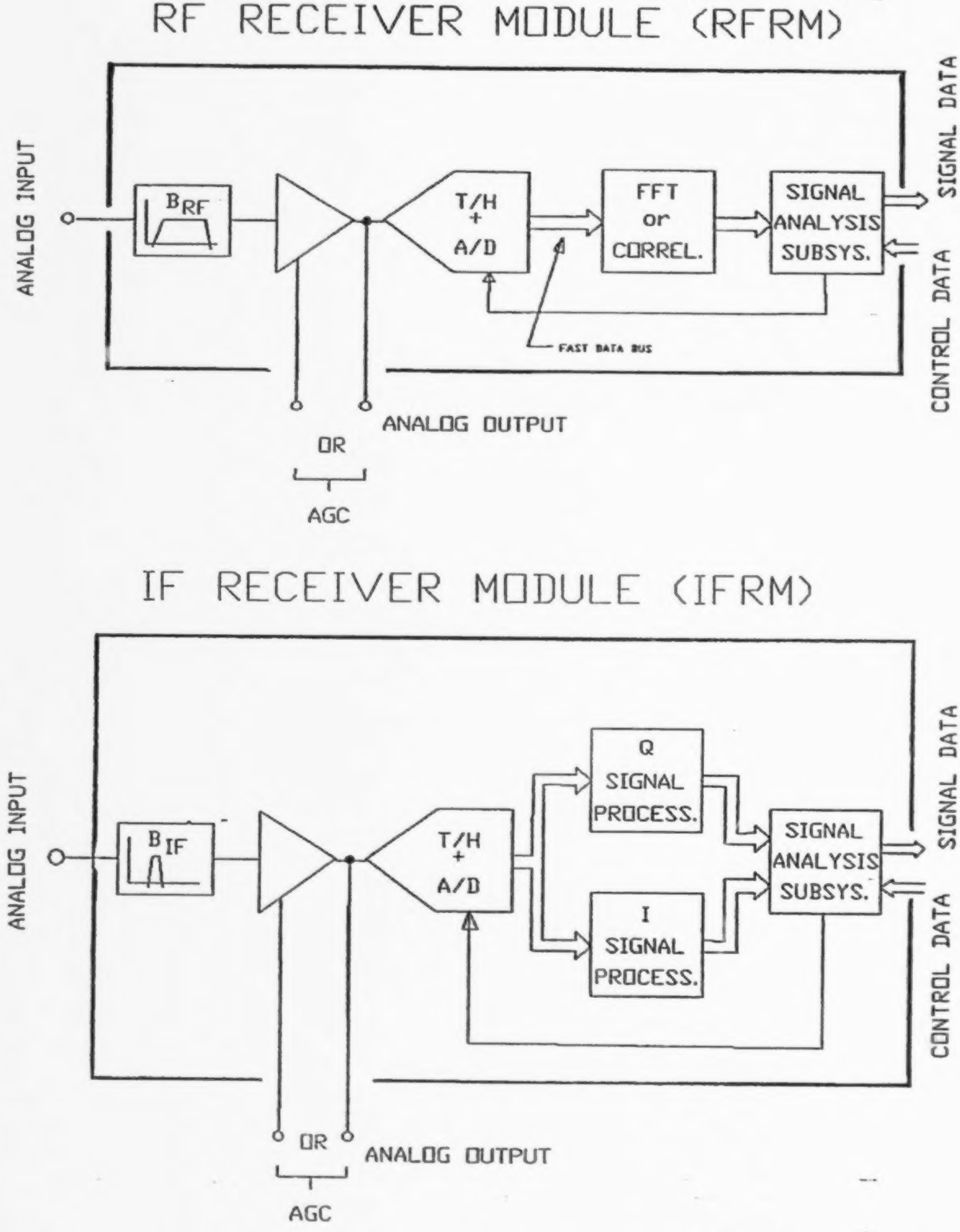
Figure 3.3.1 illustrates the two building blocks that would allow such a modularity. The need for two receiver modules exists because the receiver must cover a good portion of the communications spectrum and because most of the signal processing is done digitally in real time (real time digital processing runs at approximately 25 MHz). Therefore the RF Receiver Modules (RFRM, RF band) usually preceed the IF Receiver Modules (IFRM, IF band) in a receiver implementation.

These receiver modules will have some characteristics specified such as; input sensitivity, input bandwidth, gain, maximum processing gain, etc. So that cascading and interfacing becomes a minor task. Although the data transfer rate is fast within each individual module, it will be somewhat slower between each module and the system controller, see Figure 3.3.2.

The signal analysis sub-system in each module would be programmable to do any signal sorting and decision making under the control of the system controller.

Figure 3.3.2 illustrates a typical conceptual receiver based on this modularity architecture. Of note is the expansion capability of such an architecture. The RFRM input of receiver 01 would come from the antenna (ANT 1) or it could be a subset of another down conversion through (SY1). Also within receiver 01, there are N IFRM's each processing a channel. This is useful when the spectrum is dense and therefore more than one signal must be processed at the same time.

Another important aspect of this architecture is that, if each receiver module has it's own antenna (ie, ANT 1 to RFRM1, ANT 2 to RFRM2 etc.) then this receiver could be used also as a direction finder and again this depends on the algorithm of the system


RF RECEIVER MODULE (RFRM)

IF RECEIVER MODULE (IFRM)

FIGURE 3.3.1 RECEIVER MODULAR ARCHITECTURE

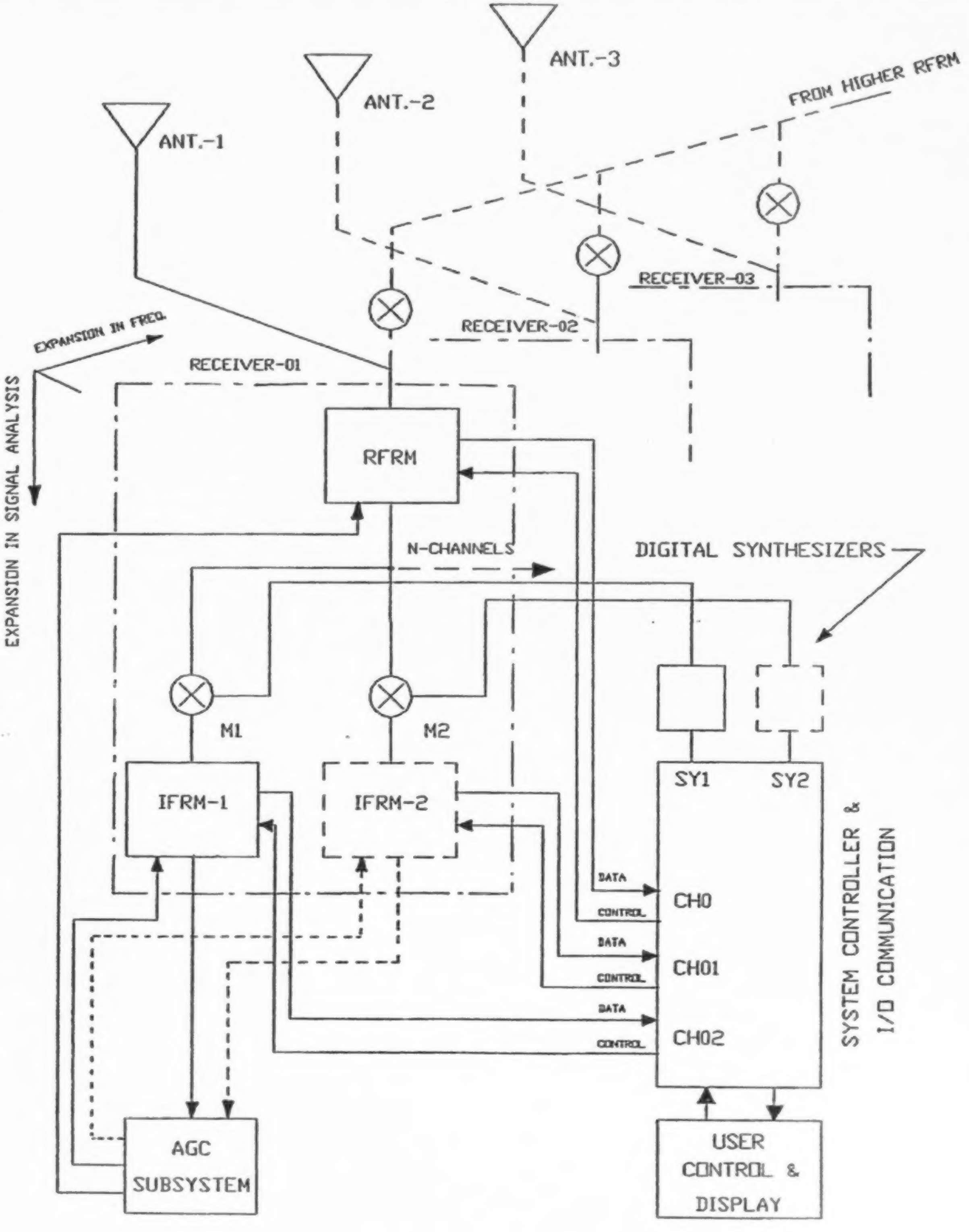


FIGURE 3.3.2 CONCEPTUAL RECEIVER BASED ON RECEIVER MODULES

controller. The system controller could be just a simple microcomputer board with some firmware capable of running different modes of operation.

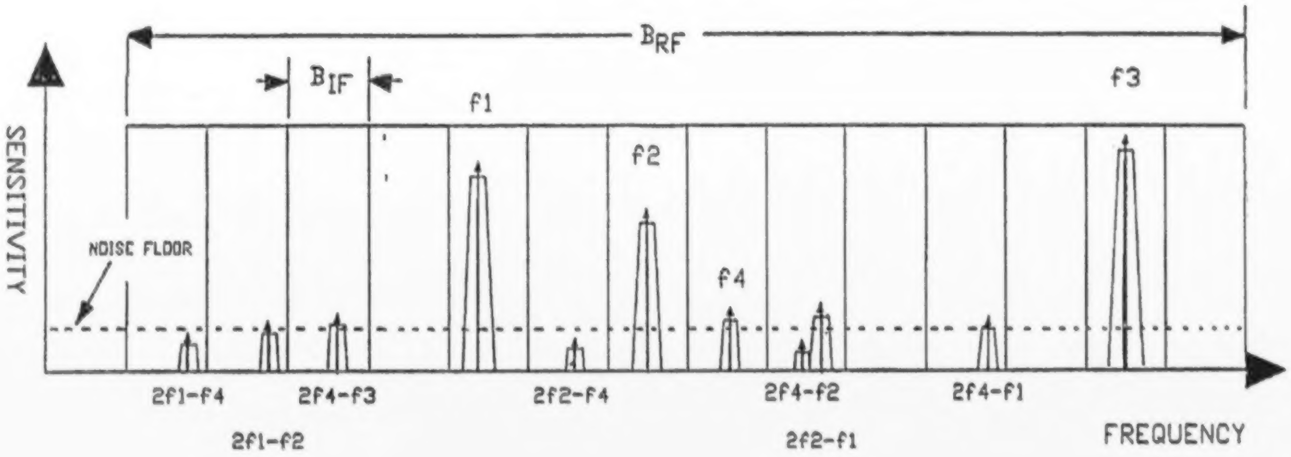
The main task of the system controller would be to analyze the signal data to determine the carrier frequency, type of modulation, sign recognition etc. and also to display all this information to a console in real time. Figure 3.3.3 illustrates a typical sequence of events that could take place on a receiver based on the modularity concept. As each module performs a little bit of processing on the signal, (concept is similar to systolic arrays), the total scan rate on the spectrum B_{RF} could be quite high thereby increasing the probability of intercept.

The modules illustrated in Figure 3.3.1 are of the hybrid type, consisting of three or four printed circuit cards enclosed in an RF shielded submodule which can be inserted into a VME type of rack, see Figure 3.3.4.

3.3 Final Considerations

To conclude this study we will draw together the information of Sections 2.1 to 2.3 and the discussion of Sections 3.1 and 3.2 in order to give a final consideration for a communication surveillance receiver system. This discussion will be based on a system intended to perform an FFT over a certain bandwidth pointing out different trade-offs that have to be made in terms of the following:

- Spurious free dynamic range
- Instantaneous dynamic range
- Sensitivity
- Instantaneous bandwidth
- Operational bandwidth
- noise figure
- Frequency resolution



① After one scan of B_{RF} module (RFRM) reports f_1, f_2, f_3, and f_4 positions to the 'system controller' (Note: the signal analysis subsystem will descriminate the true signals from intermodulation products).

② System controller assignes each (IFRM) to one signal by controling a number of digital synthesizers. The (IFRM) signal analysis subsystem will report the higher spectral resolution to the system controller for display or further processing.

FIGURE 3.3.3 SIGNAL ENVIRONMENT WITH SEQUENCE OF EVENTS OF PROCESSING IN A MODULAR RECEIVER ARCHITECTURE

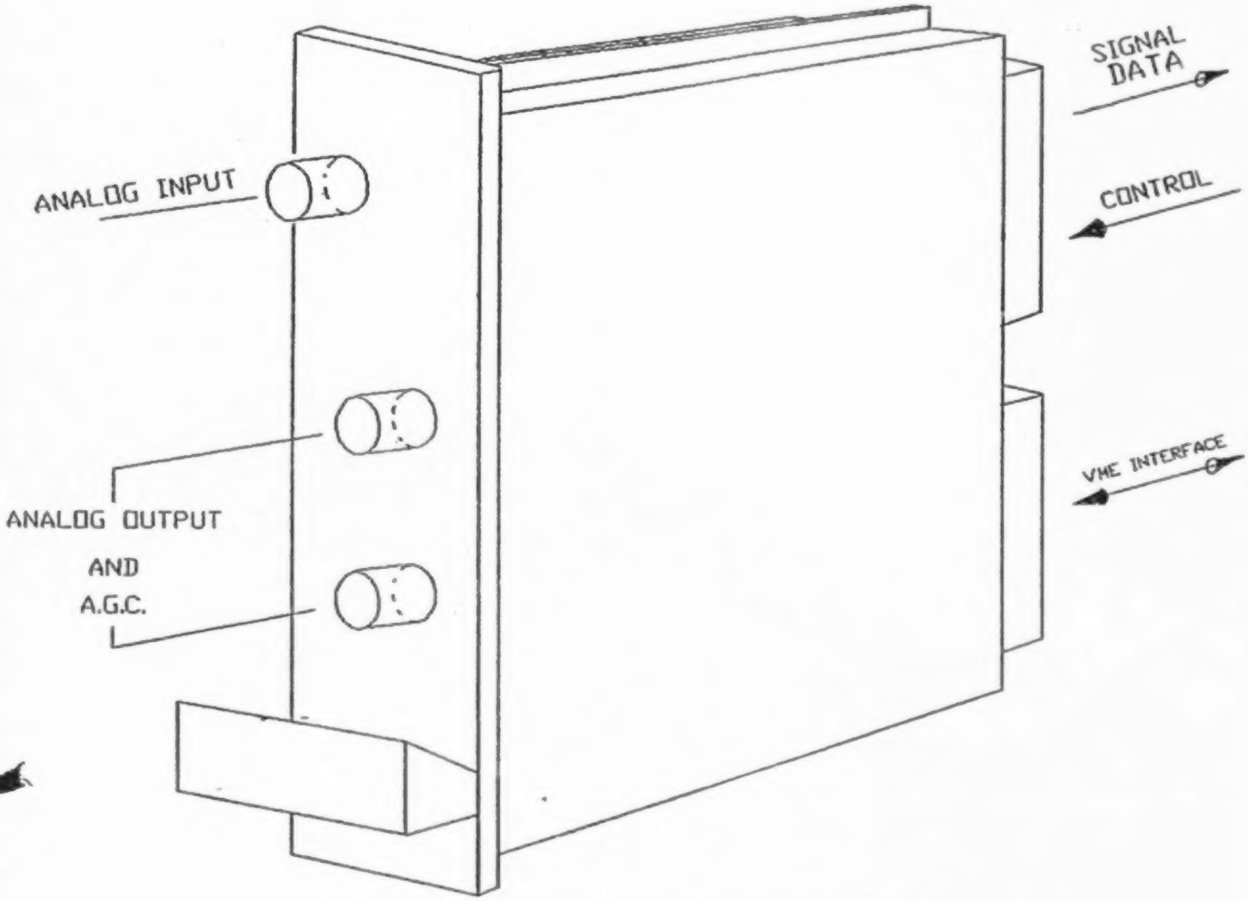


FIGURE 3.3.4 TYPICAL RECEIVER MODULE

- Performance in a multisignal environment
- Probability of RF detection
- S/N ratio.

Spurious free dynamic range: can be controlled mainly by choosing the analog devices such as amplifiers and mixers with high IIP^3 values and also by designing a sophisticated AGC sub-system which will limit the analog chain to stay on the linear transfer function, (see Figure 3.3.2). This parameter basically affects the probability of detection, but because each receiver module has a signal analysis sub-system, further digital processing of the signal can improve this probability.

Therefore the SFDR is not considered very critical in the design of the receiver system, because it can be controlled during a detailed design phase and also during digital processing.

Instantaneous Dynamic Range: can be controlled by choosing the frequency conversion component (frequency synthesizers) with the best phase noise performance. During this study it was found that digital frequency synthesizers are best suited for this application (typical phase noise -135 dBc/Hz). Also digital synthesizers settle very fast to f_{LO} (typical settling is about 10 nsec).

Therefore a careful choice of a digital synthesizer is a must in order to have a high instantaneous dynamic range which translates to a higher probability of intercept (ie, a high scan rate due to fast settling time) and also a higher probability of detection (ie, a low phase noise and therefore better definition of spectral components)

Sensitivity: this parameter is mainly dependent on technology of the analog components and also on the design of the various stages. Best results are obtained when the first stage of amplification has a very low noise figure and high gain. The sensitivity is also a function of bandwidth and processing gain.

Larger bandwidths require more processing gain for the same sensitivity level. Therefore trade-off between these two is obvious. Note that a larger instantaneous bandwidth has a higher probability of interception but higher processing gain has a lower probability of interception due to the longer scan rate. At this point, knowledge of signal levels and types would be necessary to make some compromises in the design, therefore sensitivity must be selected during detailed system analysis.

Operational Bandwidth: this is one of the system parameters which depends mostly on cost. The larger the operational bandwidth, the higher the probability of interception is. However, if only one receiver module is used, the processing time would limit the scan rate with the effect of counteracting the increase in the probability of intercept. The solution then is to use parallel processing as shown in Figure 3.3.2, where each receiver module would process a fraction of the operational bandwidth, and this is the reason why cost is higher.

Frequency resolution: would depend mainly on the size of the instantaneous bandwidth divided by the number of processing channels and by the size of the FFT processor. Higher resolution results in a high probability of detection, but increases the processing time (ie, FFT takes longer to define the spectral components) with the result of decreasing the probability of interception. Again trade-offs between instantaneous bandwidth and the size of the FFT must be made.

Signal to noise ratio: this parameter depends mainly on the number of bits used by the A/D devices. Obviously at higher frequencies we have lower S/N ratios than at lower frequencies. This can be changed only by the trend of technology. For example, in a receiver system the first processor can be used to intercept signal activity only, at a lower S/N ratio RFRM. During signal processing by the IFRM, the signal detection can be done at a higher S/N ratio, thus improving the probability of false alarm.

Performance in a multisignal environment: finally a receiver designed around the modularity concept lends itself to good performance in a multisignal environment as compared to a single receiver.

The performance will depend mainly on the sophistication of the system controller, that is the way the algorithm is designed to extract the proper information down loaded by the individual receiver modules.

4.0 FINAL CONCLUSIONS AND RECOMMENDATIONS

The study on the digital receiver has concentrated mainly on the availability of the technology and techniques for implementing a surveillance communications receiver capable of operating in the VHF band (30 MHz to 88 MHz).

During this study, considerations of the signal environment were also taken into account in order to estimate the feasibility and complexity of a receiver system. As a result, this lead us to a final conclusion which indicates that one further study should be conducted prior to the implementation of a digital surveillance receiver system.

The future work can be broken down into the following phases:

Phase-I: A detailed study of the signal environment is necessary in order to establish a baseline for the system parameters and the possible receiver architectures. The study will emphasize the following topics:

a) Frequency ranges
b) Types of emitters
    - voice
    - data
    - telemetry
    - jammers
c) Signal characteristics
    - carrier agility
    - modulation types
    - signal power
d) Associated emitters
e) Density (population distribution)

Phase-II: Based on the information in this study and on the study of Phase-I, a detailed system design will be carried out with concentration put on the following topics:

a) Detailed system design
b) Architecture trade-offs
    - performance vs. environment
    - performance vs. cost
    - cost vs. flexibility/enhancement capability
c) Detailed receiver design
    - antenna system
    - Analog front-end
    - digitizer
    - processor
    - display recording and control

Finally Phase-III would bring together all the information from the previous phases and a hardware implementation of a digital surveillance communication receiver could be initiated, followed by field trials of the prototype.

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APPENDIX A

GENERAL DATA ON BANDPASS FILTERS FROM K&L QUARTZTEK

Crystal Filters Technical Aids

Definitions

The following terms and definitions will aid you in specifying a filter for your application. An application note, "Considerations In Applying Crystal Bandpass Filters to Communications Systems" is available on request.

Passband

Insertion Loss: The loss at center frequency, normally expressed in dB, resulting from the insertion of a device in a transmission system. (Figure 2-1).

Flat Loss: The insertion loss at the frequency of minimum loss within the passband.

Attenuation: The loss of a filter at a given frequency measured in dB.

Passband (BW): The range of frequencies attenuated less than a specified value, typically 3 or 6 dB. (Figure 2-1).

Center Frequency (F_o): The arithmetic mean of the passband limits.

Fractional Bandwidth: The ratio of the passband bandwidth to the center frequency.

Reference Frequency: A specified frequency, typically the minimum loss point or F_o, from which all attenuation measurements are made.

Ripple: The amplitude difference, in dB, between the maximum passband peak and minimum passband valley. Both the peak and the valley are defined by a surrounding change in slope, i.e. sign of the amplitude response. (Figure 2-1).

Stopband

Attenuation: The output of a filter at given frequency relative to the defin insertion loss reference.

Stopband: The range of frequencies attenuated greater than some specil minimum level of attenuation. (Figur 2-1).

Transition Band (BW_T): The range ol frequencies differentially attenuated between the passband and stopban limits. (Figure 2-1).

Shape Factor: The ratio of the band at some point within the transition region, typically 60 dB, to the specifi passband bandwidth. (Figure 2-1).

Spurious Attenuation: The specified minimum level of attenuation receiv all non harmonic related resonances each crystal resonator within the filt network. (Figure 2-1).

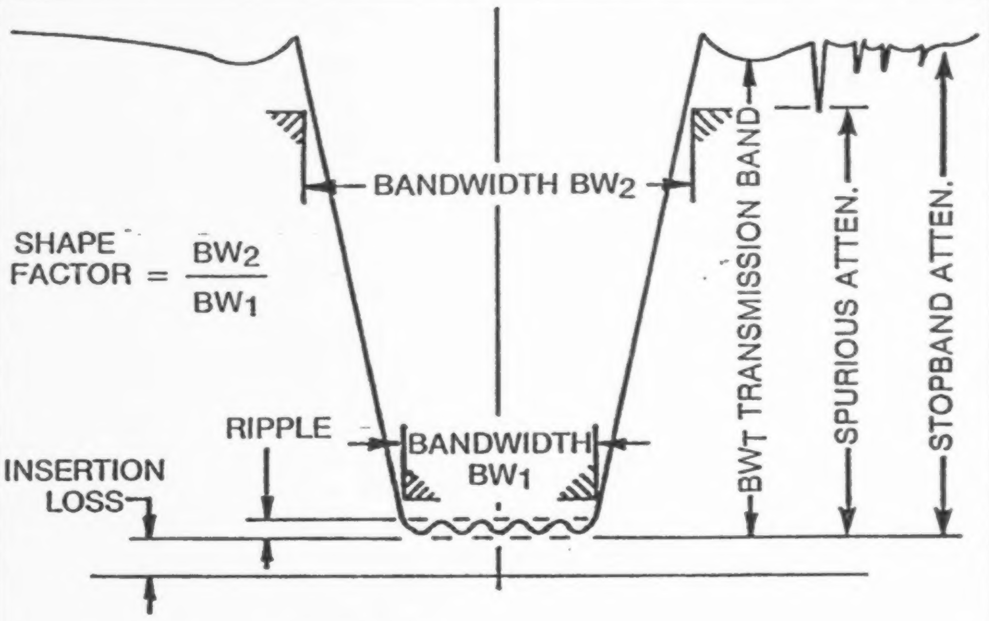


Figure 2-1. Filter Characteristics

Technical Aids Crystal Filter

Time Domain

Insertion Phase: The phase shift at the output load (measured at the reference frequency) resulting from insertion of the filter.

Differential Phase: The measurement of phase at a given frequency relative to the phase at the reference frequency.

Phase Linearity: The phase error in degrees between the phase points and the best straight line drawn through the phase points.

Group Delay: The time by which an input signal will be delayed before it appears at the filter output, i.e., the derivative of phase with respect to frequency.

Differential Delay: The measurement of delay at a given frequency relative to the reference frequency.

Source & Load Impedance

Source Impedance: The impedance of the circuit driving the filter, measured at the reference frequency.

Load Impedance: The impedance of the circuit terminating the filter at its output, measured at the reference frequency.

Non-Linear Effect

Maximum Level: The driving point power, voltage or current level above which intolerable signal distortion or damage to the device will result.

Drive Level Stability: The ability of the crystal filter to return within a specified tolerance of its original insertion loss, at a specified drive level, after experiencing changing environmental and/or drive level conditions.

Drive Level Linearity: The maximum permissable variation in insertion los per dB change in drive level, measure over a specified dynamic range.

Inband Intermodulation Distortion: Th attenuation, in dB, of 3rd and higher order signal products, inband, relative the power level of two signals placed within the passband.

Out of Band Intermodulation Distortio The attenuation, in dB, of 3rd and hig order signal products, inband, relative the power level of two signals placed the stopband, or one tone in the transition region and the other in the stopband.

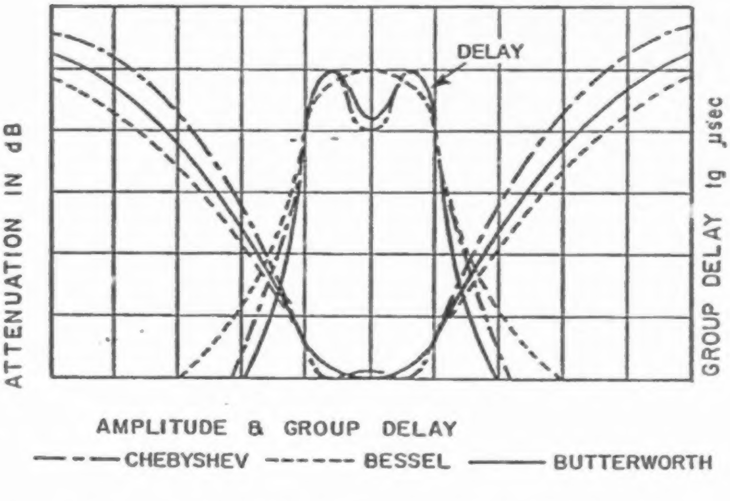


Figure 2-2. Amplitude and Group Delay of two pole Chebyshev, Butterworth and Bessel responses.

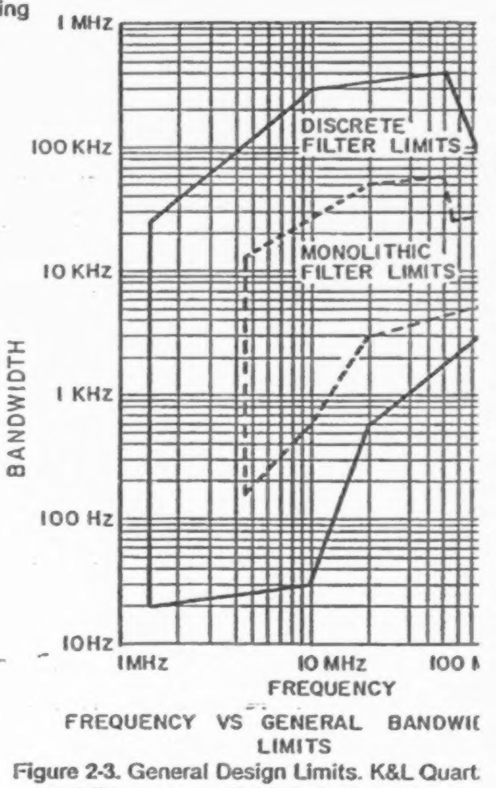
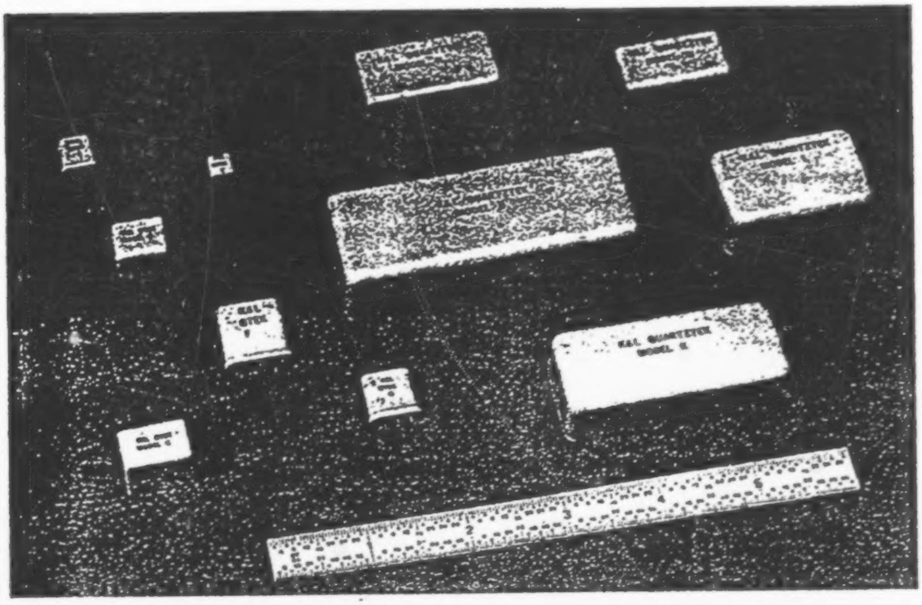


Figure 2-3. General Design Limits. K&L Quart crystal filters are available in both tandem monolithic and discrete formats. Choice of realization is a function of applicable design constraints. Approximate bandwidth limits fo K&L Quartztek filters, as a function of center frequency, are shown above.

Crystal Filters Standard Packages

1.5 MHz to 100 MHz



Standard Crystal Features

K&L Quartztek manufactures a complete line of discrete and monolithic crystal filters. Covering the frequency range from 1.5 to 100 MHz and available in 12 standard packages, these filters feature low insertion loss, good VSWR, and steep skirt selectivity.

Normal filter designs are based on a 0.01 dB Chebyshev response. Designs are realized as narrow, intermediate, or wide band, depending on fractional bandwidth requirements. Special designs available include temperature compensated, ovenized, and single sideband designs. Linear Phase, Bessel, and Gaussian family designs may be specified when improved time domain response is required.

All models may be specified to meet strict temperature, humidity, shock, vibration, and acceleration requirements.

The Selection Guide on the opposite page was designed to aid you in selecting the filter that will meet the needs of your application.

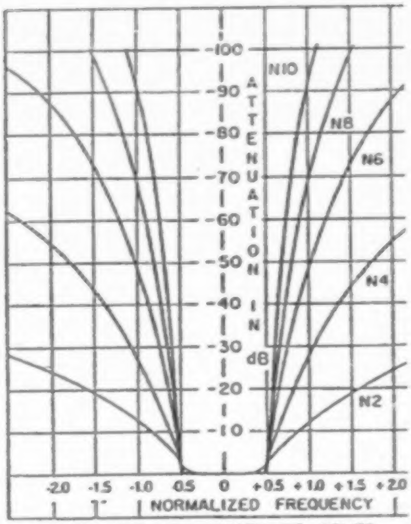
To Order

6 B H - 10.7 - 15 - P / P
1 2 3 4 5 6 7

1. Number of poles
2. Filter Type
    - B Bandpass
    - C Combset
    - D Discriminator
    - N Notch
    - O Ovenized
    - T Temperature Compensated
3. Package/Model Designation (See Pages 25,33)
4. Center Frequency or Reference Frequency in MHz.
5. Passband Bandwidth in KHz.
6. Input Connector
7. Output Connector

Mechanical

For package sizes and connector information see page 33.



SHAPE FACTOR VS NUMBER OF POLES

Figure 2-4. The normalized selectivity of K&L Quartztek 2 to 10 pole crystal filter designs is shown above.

K&L
QUARTZTE

Monolithic Crystal Filte

21.4 M

21.4 MHz Monolithic Crystal Filters

K&L Quartztek manufactures standard monolithic crystal filters in a complete range of frequencies — including 5.26, 6.46, 10.7, 16.9, and 21.4 MHz. Detailed specifications are given here for 21.4 MHz filters with channel spacings of 12.5, 20.0, 25.0, and 50.0 KHz. For specifications and information about other frequencies, contact factory.

To Order

001-39200 —
1

1. Part Number
2. Case Type

12.5 KHz Channel Spacing

P/N 001-	POLE	PASSBAND[1]		STOPBAND				LOSS	SPURIOUS	ULT. REJ.	TERM[2] (Rp/Cp)	CASE
		dB	KHz	dB	KHz	dB	KHz	dB	dB (MIN)	dB (MIN)	OHM/pF	TYPE(S)[3]
38920	2	3	±3.75	20	±18.0	—	—	2.0	12	50	850K/6	A
38940	4	3	±3.75	30	±12.5	—	—	2.5	35	70	860K/3	A(×2)[4],B,
38960	6	6	±3.75	60	±12.5	—	—	3.0	60	90	860K/3	A(×3)[4],B,
38980	8	6	±3.75	60	±10.0	80	±12.5	4.5	80	100	860K/3	A(×4)[4],

20.0 KHz Channel Spacing

P/N 001-	POLE	PASSBAND[1]		STOPBAND				LOSS	SPURIOUS	ULT. REJ.	TERM[2] (Rp/Cp)	CASE
		dB	KHz	dB	KHz	dB	KHz	dB	dB (MIN)	dB (MIN)	OHM/pF	TYPE(S)[3]
39000	2	3	±6.5	20	±30.0	—	—	2.0	12	45	1.4K/0	A,D,E
39020	4	3	±6.5	30	±22.5	—	—	2.0	35	70	1.4K/0	A,D,E(×2)[4],
39040	6	6	±6.5	60	±22.5	—	—	3.0	65	90	1.4K/0	A,D,E(×3)[4],
39060	8	6	±6.5	60	±17.5	80	±22.5	3.0	80	100	1.4K/0	A,D,E(×4)

25.0 KHz Channel Spacing

P/N 001-	POLE	PASSBAND[1]		STOPBAND				LOSS	SPURIOUS	ULT. REJ.	TERM[2] (Rp/Cp)	CASE
		dB	KHz	dB	KHz	dB	KHz	dB	dB (MIN)	dB (MIN)	OHM/pF	TYPE(S)
39080	2	3	±7.5	20	±35.0	—	—	2.0	12	45	1.6K/0	A,D,E
39100	4	3	±7.5	30	±25.0	—	—	2.0	35	70	1.6K/0	A,D,E(×2)[4]
39120	6	6	±7.5	60	±25.0	—	—	3.0	60	90	1.6K/0	A,D,E(×3)[4]
39140	8	6	±7.5	60	±20.0	80	±25.0	3.0	80	100	1.6K/0	A,D,E(×4)

50.0 KHz Channel Spacing

P/N 001-	POLE	PASSBAND[1]		STOPBAND				LOSS	SPURIOUS	ULT. REJ.	TERM[2] (Rp/Cp)	CASE
		dB	KHz	dB	KHz	dB	KHz	dB	dB (MIN)	dB (MIN)	OHM/pF	TYPE(S)
39160	2	3	±15	20	±90.0	—	—	2.0	10	40	3K/0	A,D,E
39180	4	3	±15	30	±45.0	—	—	2.0	25	60	3K/0	A,D,E(×2)[4],
39200	6	6	±15	60	±45.0	—	—	3.0	45	90	3K/0	A,D,E(×3)[4],
39220	8	6	±15	60	±33.0	80	±45.0	3.0	80	100	3K/0	A,D,E(×4)

NOTES:

1. Maximum passband ripple over operational temperature range −30° C to +80° C is: 2 pole, 1.0 dB; 4, 6, 8 poles, 2.
2. Parallel termination capacity is adjusted for optimum filter response. Nominal parallel capacity (Cp): ±3.0 pF. Impedance (Rp): Specified above.
3. See page 33 for case descriptions.
4. Multiple cases required.
   (×2) indicates that two cases are required for four pole response.
   (×3) indicates that three cases are required for six pole response.
   (×4) indicates that four cases are required for eight pole response.

K&L
QUARTZTEK

APPENDIX B

NYQUIST SAMPLING RATE

The most widely known "rule" of sampling is as follows: A band limited signal having no special components above a frequency of B Hz is determined uniquely by its values at uniform intervals spaced no greater than 1/2B seconds apart.

In simpler words, we must sample an input frequency at least twice per cycle to get a unique description of the signal. The two samples per cycle rate is known is the Nyquist Sampling Frequency, f_s. The key word in the above definition is unique. Perfectly good copies of a signal may be obtained by sampling at lower rates if we are prepared to accept additional alias copies.

The samples normally occur at a regular interval, T_s, in the time domain where, $T_s = 1/f_s$. If sampling aperture times, t_a, are very narrow then the frequency equivalent of the time domain pulse train is a frequency domain pulse train at harmonic multiples of f_s. A sampling gate is equivalent to multiplying the input signal, f_{in}, by the sampling signal. The product of the two signals is the signal output, f_p, where

$$f_p = \text{Sin} (2\pi f_{in} t) \times \sum_{n=1}^{\infty} \text{Sin} (2\pi f_s t) \qquad \text{eq.(B1)}$$

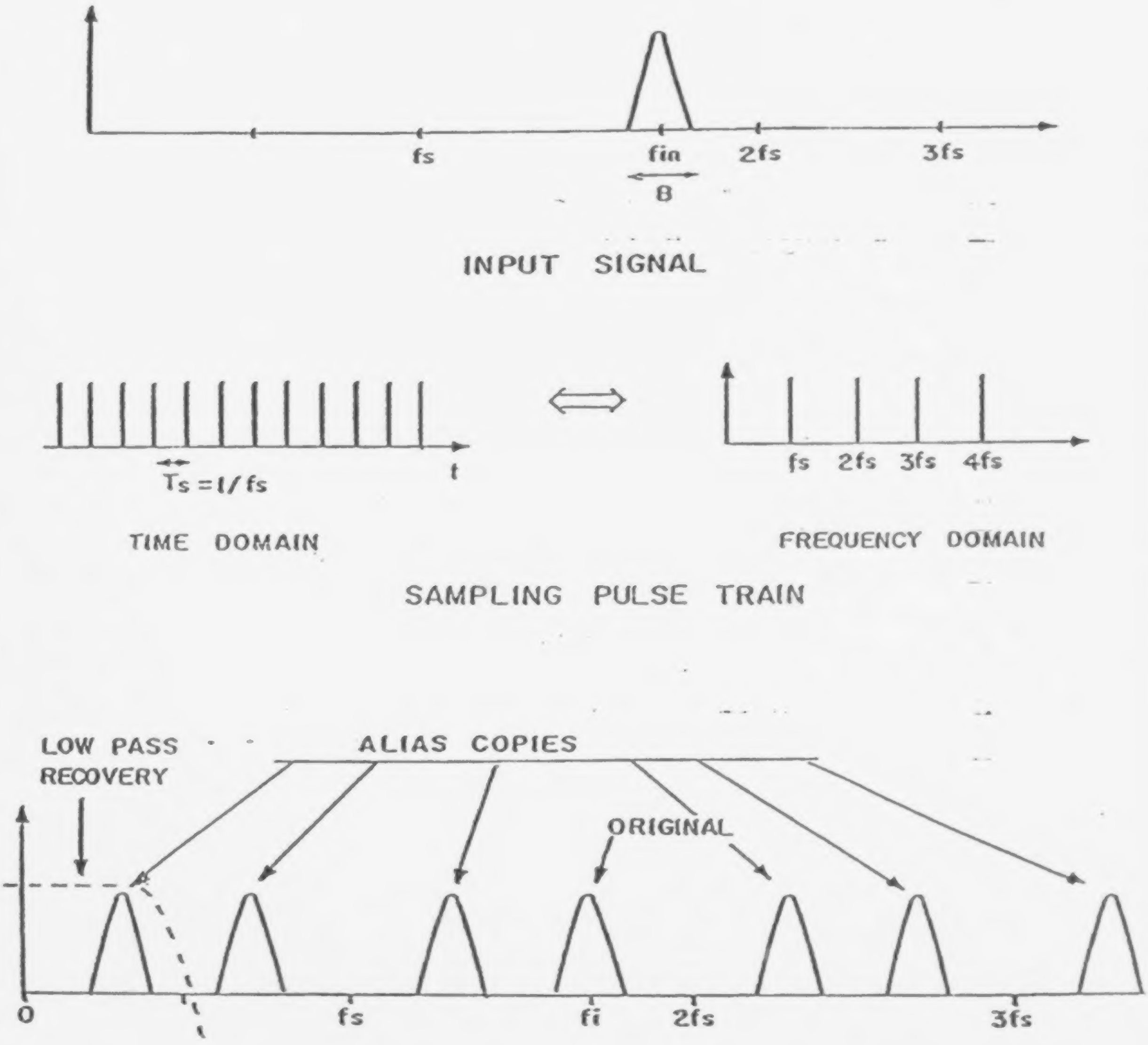
Since the product of two sinusoids results in a sum and a difference frequency we can expect alias output frequencies at

$$f_p = \text{Sin} \left[2\pi (nf_s + f_{in}) t \right] \ ; \ n = 1,2,3 \ldots \qquad \text{eq.(B2)}$$

Hence an infinite number of copies of the input signal are generated. If no apriori information is available about the input frequency range then the only way to guarantee that the baseband signals are unique is to sample at the Nyquist Rate or greater.

A key point about sampling however is that the infinite number of copies of the input signal generated by sampling, are all exact copies of the input if the sampling pulse or sampling aperture is of zero width. If the information bandwidth or baseband bandwidth B, of the input signal is less than $f_s/2$ and the center frequency is further than B/2 from any multiple of $nf_s/2$ then the alias copies will not overlap and the resulting output can be filtered to recover the input signal. This situation is illustrated in Figure B.1.

This fact is used to advantage in modern spectrum analyzers. For those who have used older spectrum analyzers without preselectors you may recall that it was necessary to identify real and false signals using the "identifier" button. The false signals were simply alias signals arising from the fact that spectrum analyzers use "harmonic" or "sampling" mixers in an undersampled mode. Modern spectrum analyzers use a preselector, which does not eliminate the alias, it merely identifies to the processor which copy of the input is the true copy. The processor then only displays the true copy. The message from all of this is that there are situations where undersampling with narrow apertures is an efficient and effective method of sampling signals. If however the bandwidth of the input signal is greater than $f_s/2$ then the alias copies will overlap and the resulting output will be corrupted, and the original signal will not be recoverable. Two possible situations in which this rule applies are illustrated in Figures B.2 and B.3.



INPUT SIGNAL

TIME DOMAIN

FREQUENCY DOMAIN

SAMPLING PULSE TRAIN

FIGURE B.1 PERFECT RECOVERY USING UNDERSAMPLING

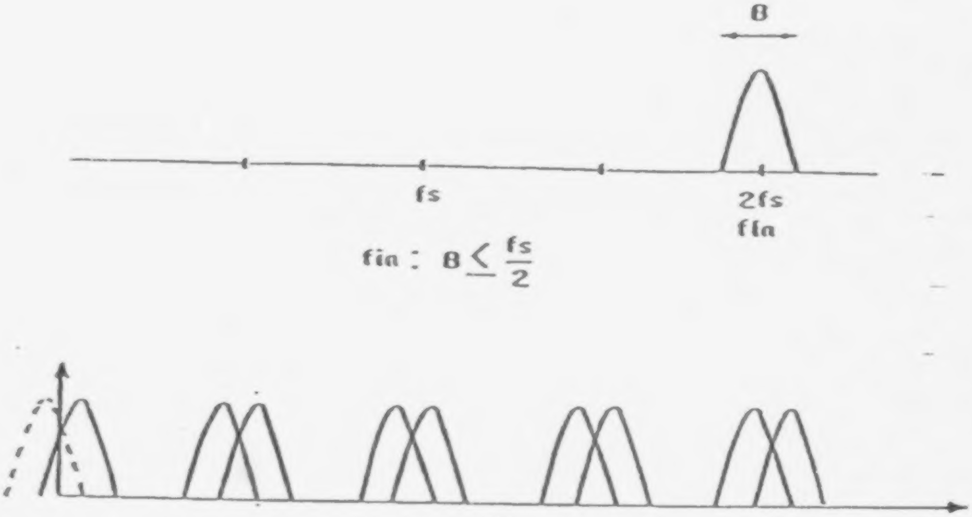


FIGURE B.2 CORRUPTED SAMPLES RESULT FROM UNDERSAMPLING OF AN INPUT SIGNAL TOO CLOSE TO n f_s /2

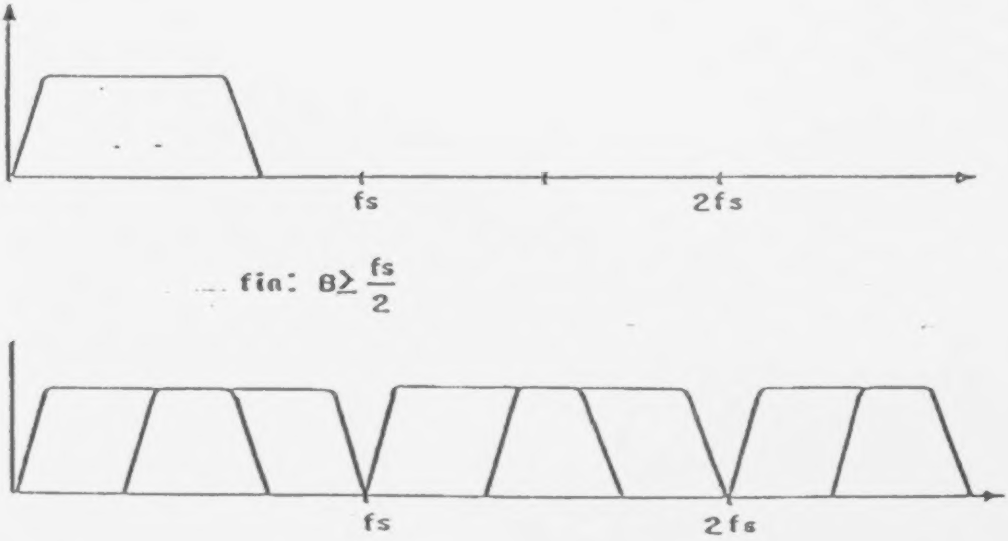


FIGURE B.3 CORRUPTED SAMPLES RESULT FROM A BESEBAND SIGNAL WITH TOO LARGE AN INFORMATION BANDWIDTH

APPENDIX C

SAMPLING APERTURE WIDTH

The sampling aperture width is of interest in practical A/D converters since obviously real sampling apertures cannot have zero width. Effectively any function, f(t), which is sampled by an aperture t_a seconds wide, is averaged for the length of time the aperture is open. Hence the voltage, V_0, seen by the sampled aperture centered at time t_0 is just

$$V_0 = 1/t_a \int_{t_0 - t_a/2}^{t_0 + t_a/2} f(t)\ dt \qquad \text{eq.(C1)}$$

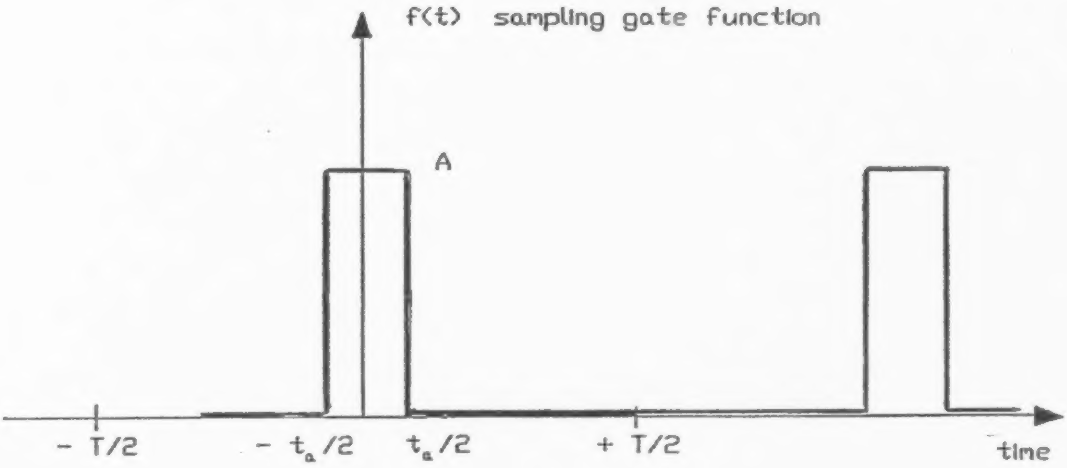
Since all functions can be expressed in terms of sinusoids it is useful to know the effect of finite aperture averaging on the input signal. Therefore, if we take the Fourier transfer function of a "sampling gate" function (see Figure C.1), i.e. we convert into the frequency domain.

$$\bar{F}_n(\bar{w}) = 1/T \int_{-T/2}^{T/2} f(t)\ e^{-jnwt}\ dt \qquad \text{eq.(C2)}$$

Solving the integral yields:

$$F_n(w) = \frac{A\ t_a}{T} \left[\frac{\mathrm{Sin}\ (\ n\ w\ t_a/2\ )}{n\ w\ t_a/2} \right] \qquad \text{eq.(C3)}$$

In the limit as the aperture width goes to zero, we see that the sampling response is flatter for a longer span on the frequency domain spectrum. Hence we get a more uniform spectral response for infinitely narrow apertures. Finite width apertures however result



TIME DOMAIN

$$F_n = \frac{1}{T}\int_{-T/2}^{T/2} f(t)\, e^{-jn\omega t}\, dt$$

FREQUENCY DOMAIN

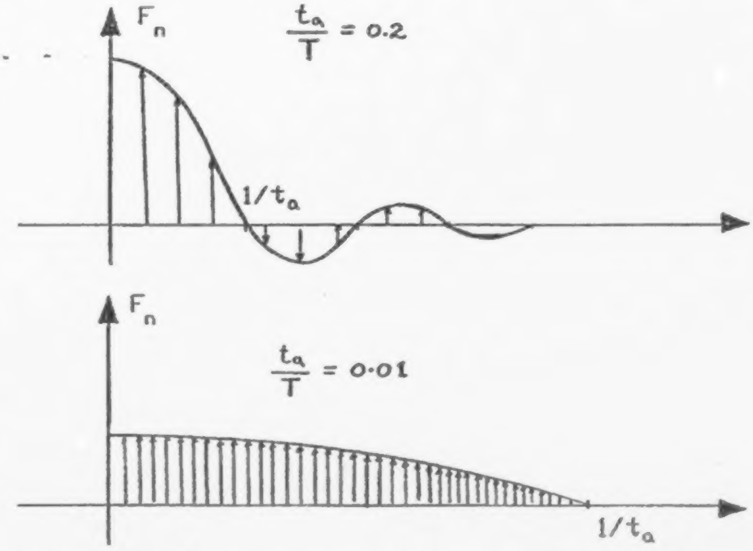


FIGURE C.1 FOURIER TRANSFORM OF A SAMPLING GATE FUNCTION

in a Sin (x)/x amplitude response versus frequency. (C.3) also yields the expected result of zero for aperture width averaging over integral multiples of a period of the input signal.

$$f_{in} = \frac{n}{t_a} \qquad V_0 = 0 \quad \text{for } n = 1,2,3 \ldots \qquad \text{eq.(C4)}$$

Table 1 gives the amplitude rolloff of the sampling function, where the signal being sampled, f_{in}, is given as a percentage of, $1/t_a = f_a$, the sampling aperture width.

f_{in} as % of 1/ta	Sampled Amplitude Response Error dB	Amplitude Response $\frac{\sin(\ f_{in} ta)}{f_{in}\ ta}$
0	0	1.00
5	- 0.04	0.995
10	- 0.14	0.983
20	- 0.58	0.935
44.2	- 3.00	0.708
60	- 5.94	0.504

TABLE -1 sampled amplitude response error versus f_{in} as a % of the inverse of the sampling aperture width, t_a

If a given A/D converter now attempts to quantize a range of input frequencies from DC to f_{max} and the A/D is an n bit quantizer, then a full scale DC input will be quantized to $1/2^n$ accuracy. The effect of a finite aperture signal averaging will prevent higher frequencies from reaching the full scale input.

The actual amplitude accuracy achieved at the input frequency will be;

$$\frac{1}{2^n}\left[\frac{\text{Sin}\ (\pi f_{in}\ t_a)}{\pi f_{in}\ t_a}\right] \qquad \text{eq.(C5)}$$

Hence a definition may be given as to the effective number of bits, n_{eff}, realized at the frequency being sampled for a given aperture width ie:

$$2^{n_{eff}} = 2^n\left[\frac{\text{Sin}\ (\pi f_{in}\ t_a)}{\pi f_{in}\ t_a}\right] \qquad \text{eq.(C6)}$$

Simplifying

$$n_{eff} = n + 3.32\ \log_{10}\left[\frac{\text{Sin}\ (\pi f_{in}\ t_a)}{\pi f_{in}\ t_a}\right] \qquad \text{eq.(C7)}$$

Some typical values of n_{eff} as a function of f_{in} and t_a are given in Table 2.

n	fin % of 1/ta	n_{eff}
8	5	7.99
8	20	7.90
8	44.2	7.5
8	60	7.01

Table 2 - n_{eff} versus fin as a Percentage of the Inverse of the Sampling Width, t_a

APPENDIX D

QUANTIFYING NOISE AND SIGNAL TO NOISE RATIO

An A/D converter quantizes the input signal to one of 2^n amplitude levels, where n is the number of binary bits used to represent each sample. The quantization process may be modelled mathematically as

$$X'_n = X_n + q_n \qquad \text{eq.(D1)}$$

where X'_n is the quantized value of X_n and q_n represents the quantization error which we will treat as additive noise. If a uniform quantizer is used having the input output characteristic shown in Figure D.1 then the noise is well characterized by the uniform probability distribution function [1], i.e. the noise is characterized by:

$$p(q) = \frac{1}{\Delta} \quad ; \text{ for } -\frac{\Delta}{2} < q < \frac{\Delta}{2} \qquad \text{eq.(D2)}$$

where the step size of the quantizer is given by: $\Delta = 2^{-n}$.
(this is assuming equal amplitude increment between levels)

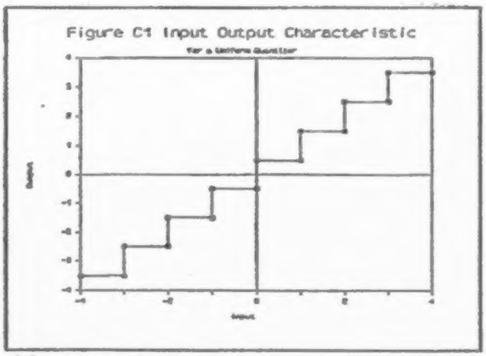


figure 1

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[1] Proakis, J.G., "Digital Communications", McGraw Hill, 1983 pp 71.

The expected value, E(q), of the quantization error is given by:

$$E(q) = \int_{-\infty}^{\infty} q p(q)\, dq \quad = \frac{\Delta}{2} \qquad \text{eq.(D3)}$$

The mean square value of the quantization error $E(q^2)$ is given by:

$$E(q^2) = \int_{-\infty}^{\infty} q^2 p(q)\, dq \quad = \frac{\Delta^2}{12} \qquad \text{eq.(D4)}$$

Once the mean square value of the noise is determined it remains to resolve the signal power to derive the S/N ratio of the quantizer.

A commonly used S/N expression [2] is derived from a signal which is assumed to have an equally probable chance of occurance at any of m quantization levels ($m=2^n$ for an n bit quantizer).

$$p(x) = \frac{1}{m}$$

The mean square of a signal with a uniform distribution is derived as follows:

$$S = \int_{-\infty}^{\infty} x^2\, p(x)\, dx$$

$$= \frac{2}{m}\left[\left(\frac{\Delta}{2}\right)^2 + \left(3\frac{\Delta}{2}\right)^2 + \quad \cdots \quad + \left[\frac{(m-1)\cdot\Delta}{2}\right]^2\right]$$

$$= \frac{(m^2 - 1)\Delta^2}{12} \qquad \text{eq.(D5)}$$

Taking the ratio of D.5 and D.4 yields:

$$S/N_{uniform} = m^2 - 1 = 2^{2n} - 1 \qquad 2^{2n}$$

$$= \quad 6n \quad dB \qquad \text{eq.(D6)}$$

While D.6 is a widely used result it is a slightly pessimistic result for quantizers used in the radar ECM world. All radar signals are sinusoidal hence the probability of occurance of the signal is more heavily weighted for the extreme values and less heavily weighted for the zero crossings.

The pdf of a sine wave is given by

$$p(x) = \frac{1}{\pi}\left[\frac{1}{\sqrt{1 - x^2}}\right] \qquad \text{for } -1 < x < 1 \qquad \text{eq.(D7)}$$

For high values of n this yields an rms signal power of:

$$S = \frac{(m - 1)^2}{\sqrt{2}}\left(\frac{A}{2}\right)^2 \qquad \text{eq.(D8)}$$

Taking the ratio of D.8 and D.4 yields

$$S/N = 1.5(m - 1)^2$$

$$\approx 6n + 1.8 \text{ dB} \qquad \text{eq.(D9)}$$

Hence as a result of quantizing sinusoids, we get a 1.8 dB advantage in S/N for large values of n. It should be noted that this approximation is in error for small values of n. For a sinusoid, the fact that states near the peak values are more probable than the states near the zero crossings doesn't affect a single bit quantizer. That is the sine wave is still 50% likely to be positive or negative. Hence, referring to D.5, the mean square signal power of a sinusoid quantized to 1 bit is given by

$$S = \int_{-\infty}^{\infty} x_2^2 \, p(x) \, dx \qquad ; n = 1, m = 2$$

$$= \left(\frac{A}{2}\right)^2 \qquad \text{eq.(D10)}$$

Taking the ratio of D.10 and D.4 yields the S/N ratio for a sinusoid quantized to 1 bit:

$$S/N = 3 \qquad \approx \qquad 4.8 \text{ dB} \qquad \text{eq.(D11)}$$

As expected this is the identical result to the equiprobable state case.

As a second example, we see a 0.9 dB advantage in a 3 bit quantizer, ie. n=3, m=8. Hence, referring to D.5, we get;

$$S = \int_{-\infty}^{\infty} x^2 \; p(x) \; dx$$

$$= \frac{2}{8}\left[0.09\left[\frac{\Delta}{2}\right]^2 + .1\left[\frac{3\Delta}{2}\right]^2 + .14\left[\frac{5\Delta}{2}\right]^2 + .17\left[\frac{7\Delta}{2}\right]^2\right]$$

$$= 25.64\left(\frac{\Delta}{2}\right)^2 \qquad \text{eq.(D12)}$$

Dividing D.12 by D.4 yields the S/N ratio for a sinusoid quantized to 3 bits:

$$S/N = 25.64\ (3) \cong 18.9\ \text{dB} \qquad \text{eq.(D13)}$$

The differences between the actual and approximate S/N formulas for the equiprobable and sinusoid inputs are given in Table D1.

n	$S/N_{UNIFORM}$ $10\log(2^{2n}-1)$	$S/N_{UNIFORM}$ APPROX 6n dB	S/N_{SINE} ACTUAL	S/N_{SINE} APPROX 6n + 1.8 dB
1	4.8	6.0	4.8	7.8
2	11.8	12.0	12.0	13.8
3	18.0	18.0	18.9	19.8
4	24.1	24.0	25.3	25.8
8	48.2	48.0	49.9	49.8

Table D.1

The major points are:

a) don't use the approximate formulas for 1 bit S/N
b) the uniform distribution is pessimistic by 1.8 dB for large n.

It should be noted that this signal to noise ratio formula is specified for the theoretical expected wide band noise power. This formula makes no predictions as to the signal to any individual frequency ratio on a hertz by hertz basis, except to say that theoretically it should be better than 6 dB/bit + 1.8 dB. Actual A/D converters are somewhat worse than this formula. Many manufacturers do not specify the S/N ratio for their A/D converter, while others will only give it at a very low input frequency and clock frequency. Sometimes quantizing uncertainty or quantizing error is given. The inherent quantizing error of an A/D converter is usually given as a fraction of the least significant bit (LSB), Ne. This number may be related to the S/N ratio by considering the following approximation. When a full scale sinusoid is applied to an A/D input with additive noise present the A/D sees Signal + Noise and quantizes the signal at 2^n-1 (/2). Hence the mean square signal + noise power is given by:

$$S + N = \frac{(2^n - 1)^2}{\sqrt{2}} \left[\frac{\Delta}{\cdot 2}\right]^2 \qquad \text{eq.(D14)}$$

The noise error, or quantizing accuracy N_e, is given as a fraction of the LSB, and adds out of phase with the input signal in a random fashion. This is illustrated in Figure D.2. If the noise power is assumed to have a uniform distribution then the RMS noise power is given by

$$\mathrm{RMS}_{\mathrm{NOISE\ POWER}} = \frac{(N_e \Delta)^2}{\sqrt{3}} \qquad \text{eq.(D15)}$$

hence the ratio of D.14 and D.15 yields

$$\frac{(S + N)}{N} = \frac{3}{8} \frac{(2^n - 1)^2}{{N_e}^2}$$

$$S/N \approx 6n - 4.3 - 20\log N_e \qquad \text{eq.(D16)}$$

If Ne = ± ½ LSB then D.16 yields the expected result given in D.9.

It should be reemphasised that equation D.16 is an approximate evaluation of the effect of the quantizing error on the S/N ratio, which may be used only to compare manufacturers claims of quantizing accuracy, N_e, with expected S/N ratios.

As an example given a 8 bit quantizer where the manufacturer claims ± ½ lsb quantizing error then we can expect

$$S/N \quad 6\,(8)+3 - 20\log(.5) = 49.7\ \mathrm{dB} \qquad \text{eq.(D17)}$$

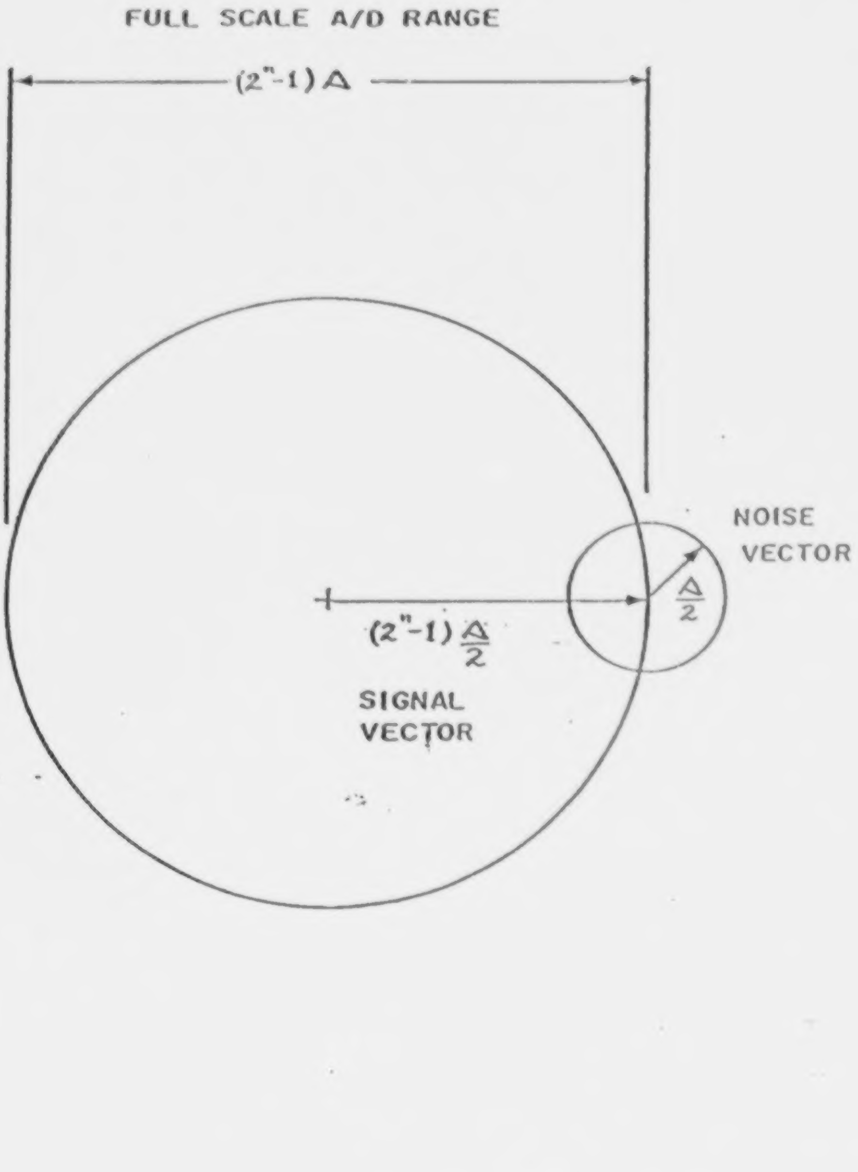


FIGURE D.2 SIGNAL AND NOISE IN AN A/D

APPENDIX E

APERTURE JITTER

It is clear that if the sampling aperture opens at a point in time other than at the time required for the desired sample then an error may occur. The possibility of error is related to two factors. The first factor is the rate of change of the input signal. Obviously if the signal doesn't change then we can open the aperture at any time without error. If the signal is changing however and we are attempting to quantize the signal to 1 part in 2^n then we must open the aperture within certain limits. Figure E.1 illustrate a sinusoid of frequency f being sampled at its point of maximum slope. If the error resulting from the aperture jitter is to be kept below the LSB error then the aperture jitter, t_{aj}, must be less than $\pm 1/(2^{n+2} f)$.

Sources of aperture jitter arise from clock phase noise, semiconductor thermal noise and EMI interference to name a few. If it is assumed that for an n bit A/D, sampling at a period of T, with highest input frequency of period 2T, then the maximum allowable aperture jitter is just

$$t_{aj} = \pm \frac{T}{(2^{n+1})\pi} \qquad \text{eq.(E1)}$$

This represents a required stability, T', from the sampling clock of

$$T' = T \pm t_{aj} \qquad \text{eq.(E2)}$$

Hence the short term clock stability must be better than $1/2^{n+1}$ to ensure no bit errors. It should be noted that oscillator stability is normally quoted in terms of one standard deviation from the carrier, hence to ensure a low probability of a bit error one should choose a clock oscillator with short term stability an order of magnitude greater than $1/2^{n+1}$, ie. at least $0.1/2^{n+1}$. A better way to choose the oscillator is via the phase noise better way to choose the oscillator is via the phase noise performance. The phase noise of the clock when viewed on a spectrum analyzer is a representation of the percentage of time the clock oscillator spends at a given frequency vs the center frequency. If for example we have a 10 MHz clock in a 12 bit system then according to E.2, we need an absolute stability of 38 ppm. This represents ±388 Hz at 10 MHz. If we require less than 1 bit error per million samples then the clock phas noise requirements would be -60 dBc/Hz at 770 Hz from the carrier.

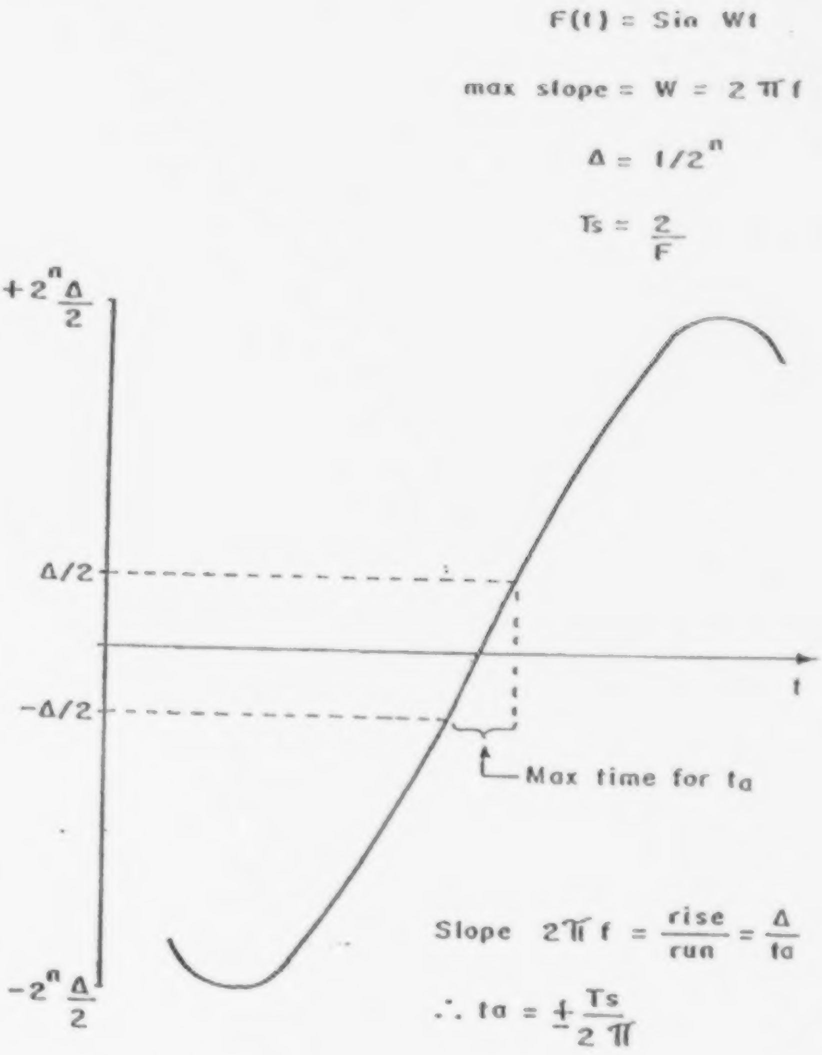


FIGURE E.1 APERTURE TIME FOR A 1 BIT ERROR

APPENDIX F

DYNAMIC PERFORMANCE TESTING OF A/D CONVERTERS

DYNAMIC PERFORMANCE TESTING OF A TO D CONVERTERS

How many sports car enthusiasts would buy a sports car based solely on engine displacement or number of cylinders? Probably none. The sports car enthusiast realizes that road performance has little to do with these hardware specs. He would probably insist on some dynamic performance data, such as acceleration tests, slalom tests, or time for the standing quarter mile. Fortunately for the performance-minded car buyer, dynamic performance data on most any car is readily available.

Sadly, this situation doesn't exist in the world of A to D Converters. Too many users of A/D's rely on hardware spec's such as number of bits or maximum sample rate when they really need a dynamic performance measure.

In fact, if there are any performance spec's on an A/D, they're generally only valid for static inputs. But real world signals are rarely static—they're dynamic. The job of the A to D Converter is to provide an accurate digital representation of the "instantaneous" amplitude of the changing input signal at precise sample times. Errors occur because the sample is taken at the wrong time (aperture uncertainty) or because the output code is not the correct representation of the signal amplitude at the sample time. These errors produce distortion in the digital representation of the signal waveform as seen in Figure 1.

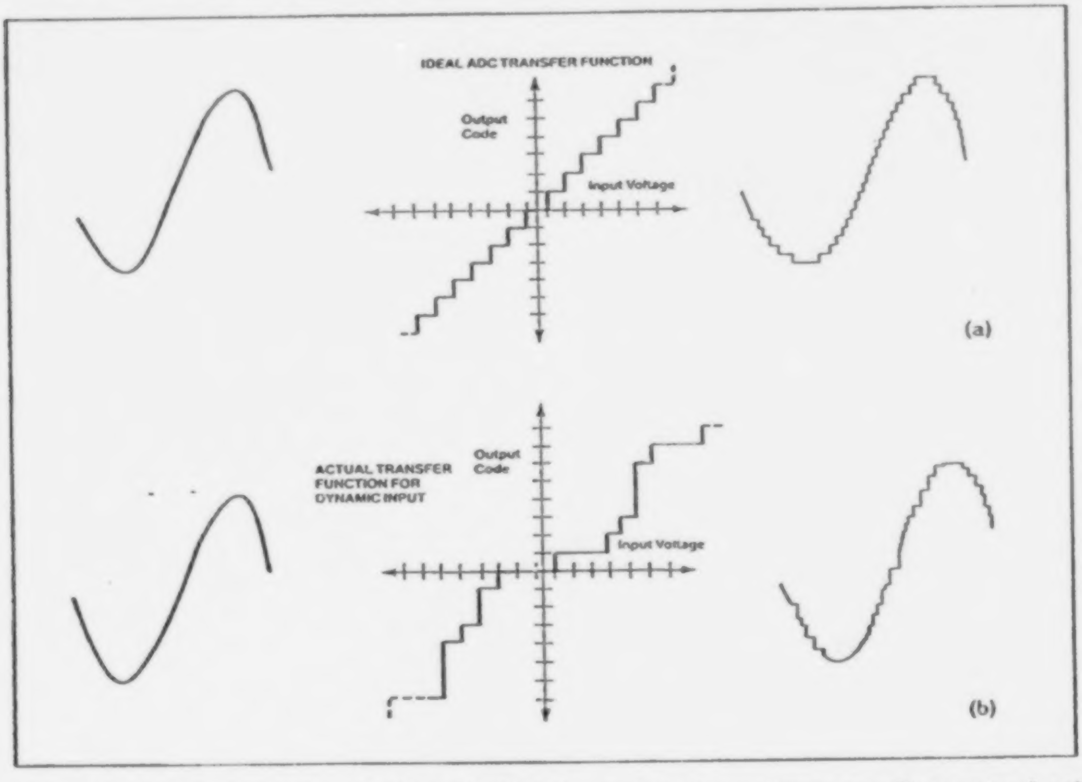

IDEAL ADC TRANSFER FUNCTION
Output Code
Input Voltage
(a)
ACTUAL TRANSFER FUNCTION FOR DYNAMIC INPUT
Output Code
Input Voltage
(b)

Figure 1(a). The distortion in the output for an ideal ADC is entirely due to quantization error. The error is reduced for an ADC with more bits. **1(b).** The distortion in the output for an actual ADC with dynamic input results from differential nonlinearities, integral nonlinearity, aperture uncertainty and noise.

There are many reasons why an ADC with N bits doesn't perform like an ideal N bit converter under dynamic operating conditions. The often wide discrepancy between dynamic and static performance is caused mainly by response time, settling time, and slew rate limitations of active devices used in the ADC as well as ADC timing jitter (aperture uncertainty).

To adequately describe the dynamic performance of the 10 bit, 20 MHz A/D Converter in Hewlett-Packard's 5180A Waveform Recorder, a number of dynamic performance tests were devised utilizing full scale sinewaves as the reference signal. These tests are sensitive to the following dynamic errors: differential nonlinearities, integral nonlinearity, aperture uncertainty, and noise.

Although some users may object to the idea of using sinewaves as reference signals on the grounds that the signals they usually digitize are transient waveforms, a sinewave reference has a number of distinct advantages: it's reproducible—this means that test results may be duplicated and verified using any number of readily available high quality sinewave generators (there are no reproducible transient generators in widespread use); it's easily characterized—a sinewave is simple to describe mathematically and its characteristics are well known, especially the very important parameter of slew rate. Sinewaves are also bidirectional which means that a sinewave test signal will pin point A/D problems that depend upon the slope (+ or −) of the input signal.

For dynamic test purposes, it's important to use full scale sinewaves as test signals. Signals which are less than full scale can produce misleading results, especially when test results are expressed as if a full scale signal were used. Misleading results can occur for two reasons: 1) if a half amplitude sinewave is used, then only ½ the possible codes are tested. Specifying performance relative to full scale assumes that the remaining 50% of the codes behave identically to the codes tested; 2) worse than this, however, is the fact that ADC performance is generally slew rate limited. A full scale sinewave has twice the slew rate of a half scale sinewave at the same frequency. Performance for a half amplitude sinewave at a specified frequency is, therefore, overstated when compared to a full scale sinewave at the same frequency.

The dynamic tests covered in this note are: histogram testing, Fast Fourier Transform (FFT) Testing, sinewave curve fitting, and beat frequency testing. All these tests use full scale sinewaves as the test signal. These tests have been selected because they give a better understanding of ADC performance as it relates to dynamic, real-life measurement situations. Since the tests are easily performed using readily available test equipment and controllers, dynamic operation can be easily verified for increased measurement confidence.

Annotated listings of all software are provided in Appendix IV.

HISTOGRAM TESTING

In the histogram test, a full scale sinewave of specified frequency is input to the ADC under test. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A to D Converter. Several hundred thousand samples of the input signal are taken and processed by the histogram software (see flowchart in figure 2). As few as 20,000 samples may be taken without significant degradation in the repeatability of the measurements. At the end of sampling, the histogram is plotted with possible output codes along the X axis and frequency of occurrence along the Y axis. Above each possible output code (for a 10 bit ADC, the X axis extends from 0 to 1023), a point is plotted whose height is proportional to the total number of times that code occurred. For a sinewave input, a perfect ADC would produce the familiar cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi\sqrt{A^2 - V^2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. Likewise, a step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 3). Figure 4 shows histograms for the 5180A at test frequencies of 0.95 MHz, 4.95 MHz, and 9.85 MHz. Figure 5 shows histograms of some other waveform digitizer products using A/D's with specified sample rate greater than or equal to 20 MHz.

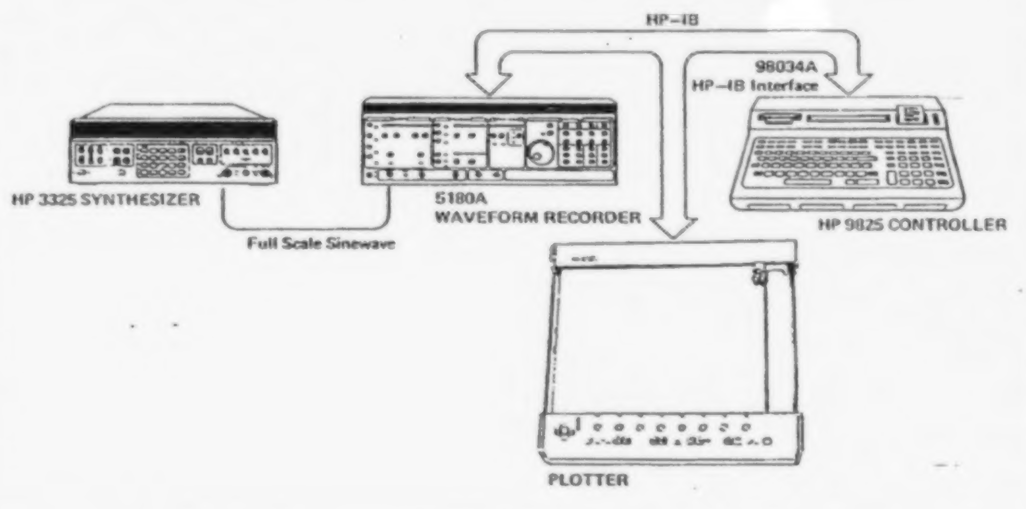


Figure 2A. Measurement set-up for histogram test.

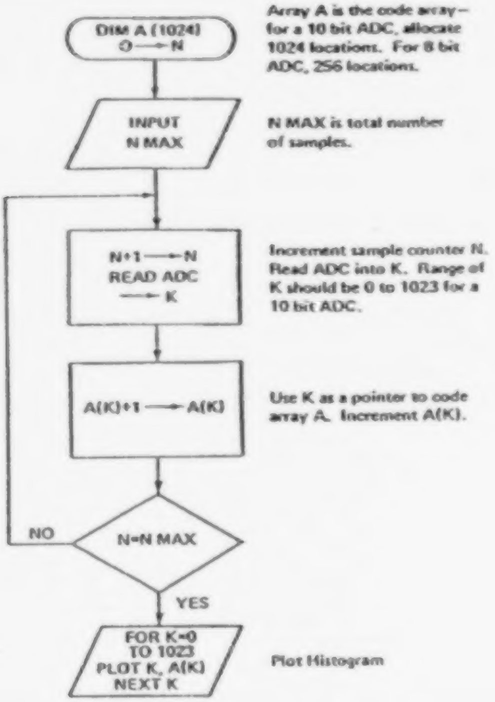

DIM A (1024)
0 → N
Array A is the code array—for a 10 bit ADC, allocate 1024 locations. For 8 bit ADC, 256 locations.
INPUT
N MAX
N MAX is total number of samples.
N+1 → N
READ ADC
→ K
Increment sample counter N. Read ADC into K. Range of K should be 0 to 1023 for a 10 bit ADC.
A(K)+1 → A(K)
Use K as a pointer to code array A. Increment A(K).
NO
N=N MAX
YES
FOR K=0
TO 1023
PLOT K, A(K)
NEXT K
Plot Histogram

Figure 2B. Flow chart for histogram program.

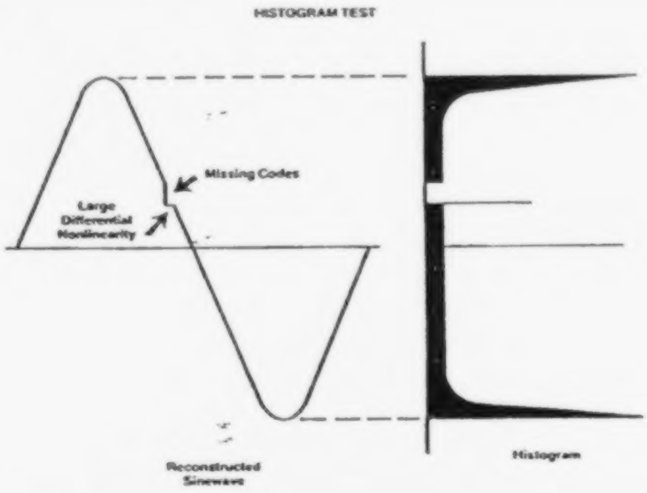


Figure 3. In the histogram test, ADC transfer function step widths larger than ideal show up as spikes in the histogram. Codes missing from the transfer function show up as bins with zero counts.

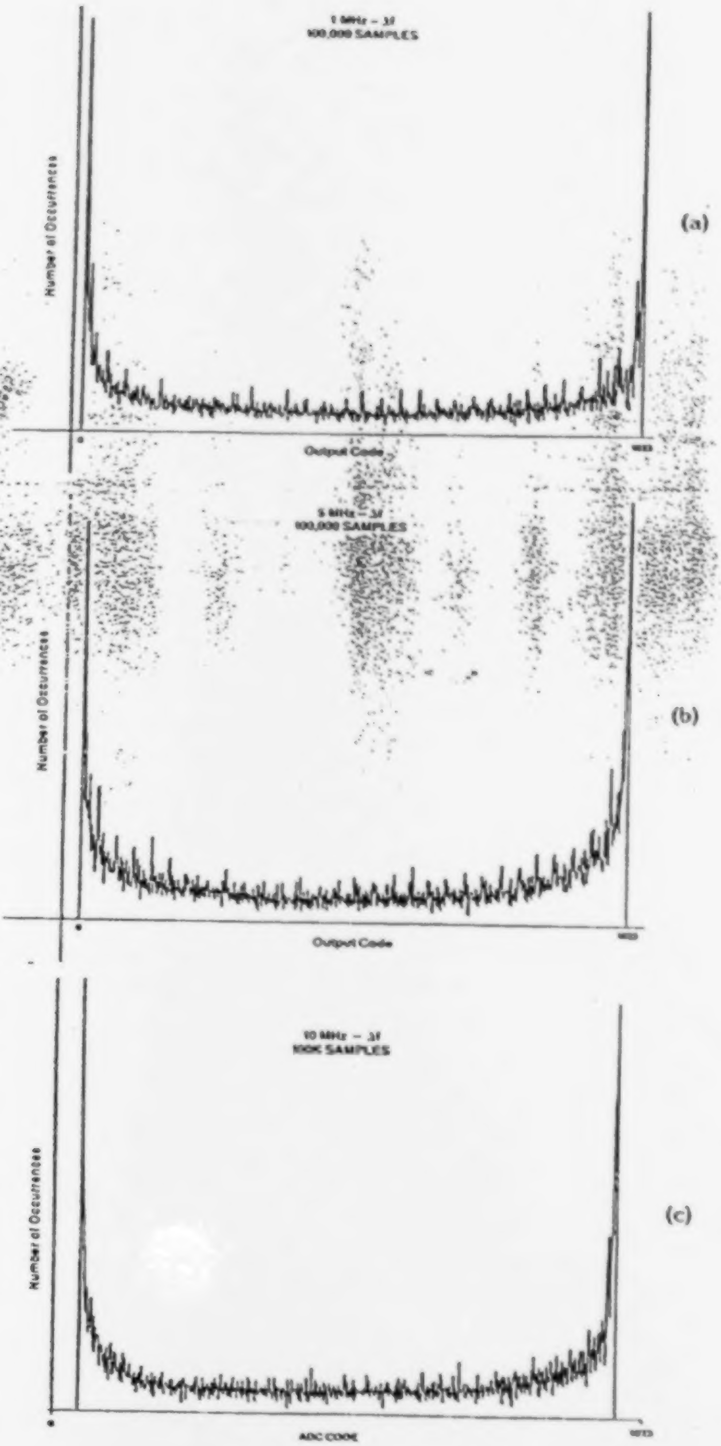


Figure 4. Histogram plots for the 20 MHz, 10 bit ADC used in the HP 5180A. The frequency in (a) is 0.95 MHz; (b) 4.95 MHz; (c) 9.85 MHz. Absence of large spikes indicates small differential nonlinearity. There are no missing codes since no points fall on the X axis.

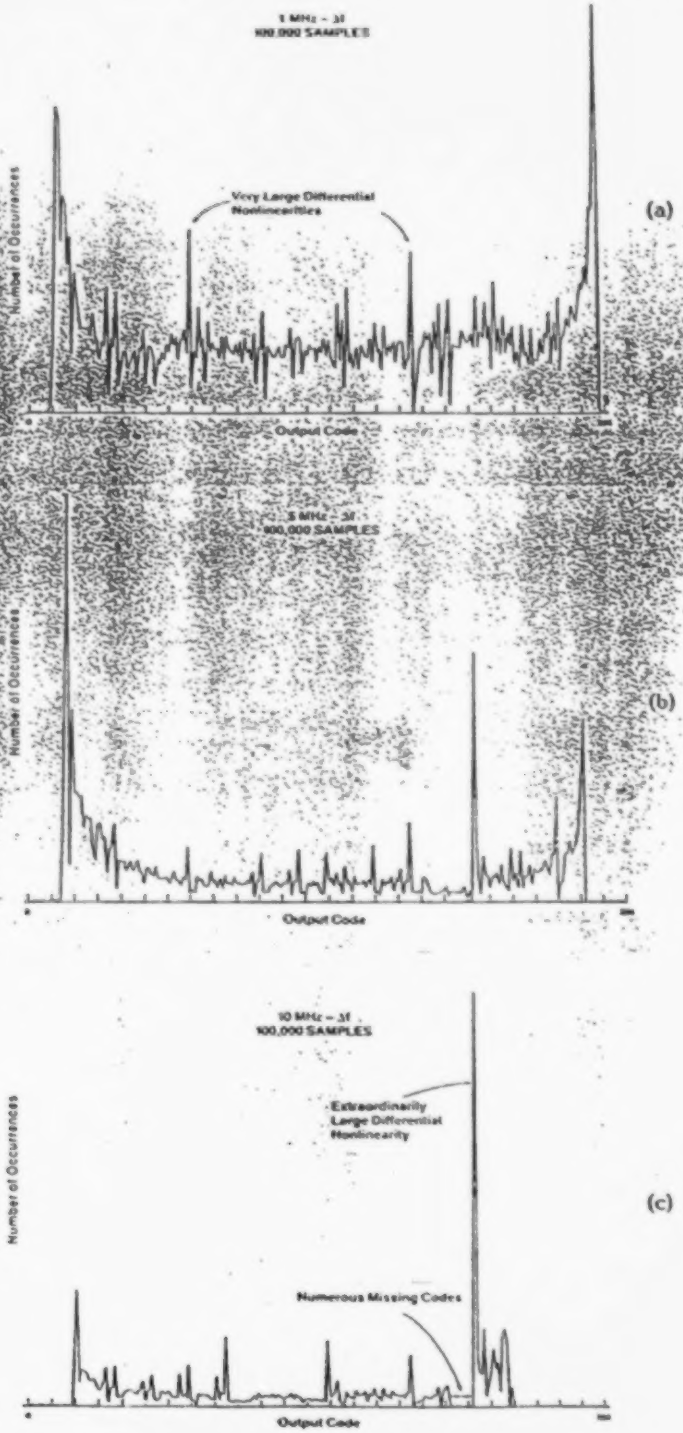


Figure 5. Histogram plots for a 20 MHz, 8 bit ADC. The frequency in (a) is 0.95 MHz, (b) 4.95 MHz, (c) 9.85 MHz. Large differential nonlinearities are apparent in all three plots. Also apparent are numerous missed codes

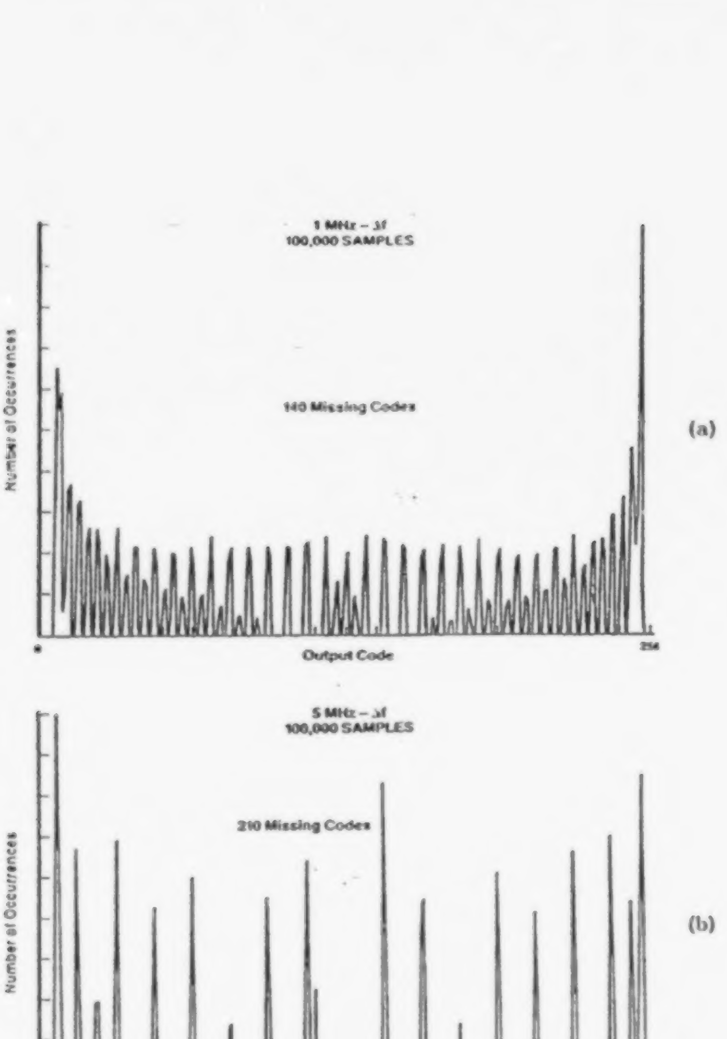


Figure 5 (cont'd). Histogram plots for a 100 MHz, 8 bit ADC. Sample rate used was 20 MHz. Frequency in (a) is 0.95 MHz; (b) 4.95 MHz; (c) 9.85 MHz. Extremely large differential nonlinearities and numerous missed codes are apparent.

The histogram test also detects gain and offset errors. For a zero offset sinewave input, the histogram should be symmetrical about the ADC output code corresponding to midscale. Large gain errors can be detected by looking at the width of the histogram.

For a perfect ramp input signal, the width of any quantization step may be computed from

$$Q_i = \frac{V\,x_i}{X}$$

Q_i = $_i$th quantization step width
V = peak-to-peak full scale range of the ADC
x_i = number of counts in the $_i$th code
X = total number of samples.

By subtracting the ideal step width from Q_i, the differential nonlinearity of each code transition can be plotted. For a sinewave input, it's still possible to compute differential nonlinearity by making a small correction for the fact that the input is a sinewave and not a perfect ramp. The following equation, based on the probability density function for a sinewave, computes the probability of occurrence of the $_i$th code in the ADC transfer function:

$$P({}_i\text{th code}) = \frac{1}{\pi}\left(\sin^{-1}\left[\frac{V\,(I - 2^{N-1})}{A2^N}\right] - \sin^{-1}\left[\frac{V\,[(I-1) - 2^{N-1}]}{A2^N}\right]\right)$$

Where V = full scale range of the ADC
N = number of bits in the ADC
I = code (offset binary coding only); for the 10 bit 5180A, codes range from 0 to 1023
A = peak amplitude of the input sinewave (The 5180A uses a slightly larger than full scale sinewave)

The differential nonlinearity (in LSB) is then computed from:

$$\text{diff nonlinearity (LSB)} = \frac{\text{actual probability } ({}_i\text{th code})}{\text{ideal probability } ({}_i\text{th code})} - 1 = \frac{x_i/X}{P\,({}_i\text{th code})} - 1$$

Figure 6 shows differential nonlinearity plots for the HP 5180A.

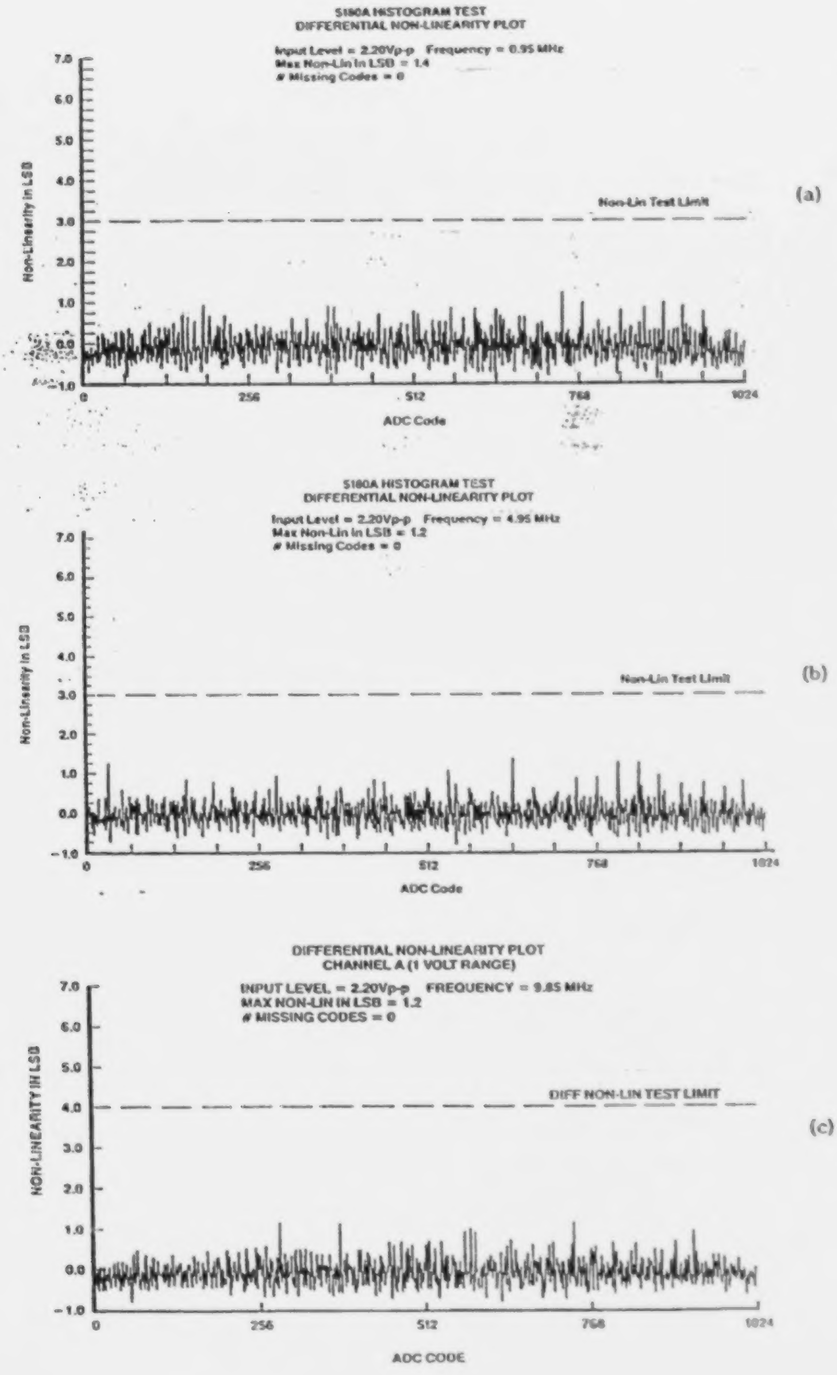


Figure 6. Differential nonlinearity plot for the 5180A at 1, 5 and 10 MHz input signals. Maximum differential nonlinearity is shown to be less than 1.2 LSB at 10 MHz.

APERTURE UNCERTAINTY AND THE LOCKED HISTOGRAM TEST

One of the most abused specifications found on the typical ADC data sheet is aperture uncertainty. In general, no test exists for this specification and the number specified is simply a "good faith" guess. A variation of the histogram test, called the "locked" histogram, may be used to estimate aperture uncertainty and noise. In this test, the encode signal to the A to D Converter must be synchronized ("locked") to the test signal being digitized. The test set-up for testing the 5180A is shown in Figure 7 and uses an external timebase to synchronize the input signal with the sample command. (It's important that the external timebase used have significantly less jitter than the aperture uncertainty you're trying to measure—the HP 8640B has extremely low phase noise: −140 dB below carrier in a 1 Hz bandwidth at frequencies greater than 100 kHz from the carrier. This is equivalent to sample to sample jitter of approximately 12 picoseconds at a 20 MHz encode rate.)

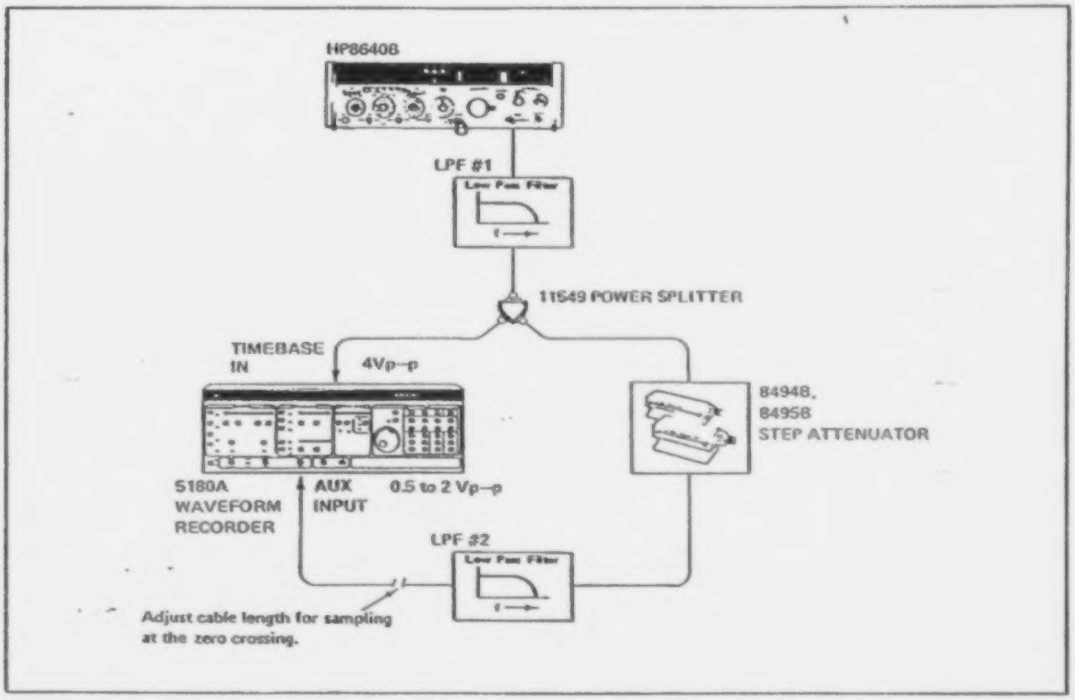


Figure 7. Test set-up for measuring aperture uncertainty and noise.

Since the sample command and the signal being sampled are "locked" together, a perfect ADC with zero noise and no timing uncertainty would sample at precisely the same point on the test signal each and every time. The result of noise and timing jitter is to cause the sample point to vary. By taking several hundred thousand samples and producing the histogram plot, the aperture jitter and noise may be estimated. Figure 8 shows locked histogram plots at various sinewave frequencies and amplitudes. It's apparent that at higher slew rates, the spread of the histogram increases. The standard deviation of the histogram provides an rms estimate of the amount of spread in terms of the LSB. Aperture uncertainty is directly proportional to slew rate while noise is that portion of the spread which is constant and doesn't change with slew rate.

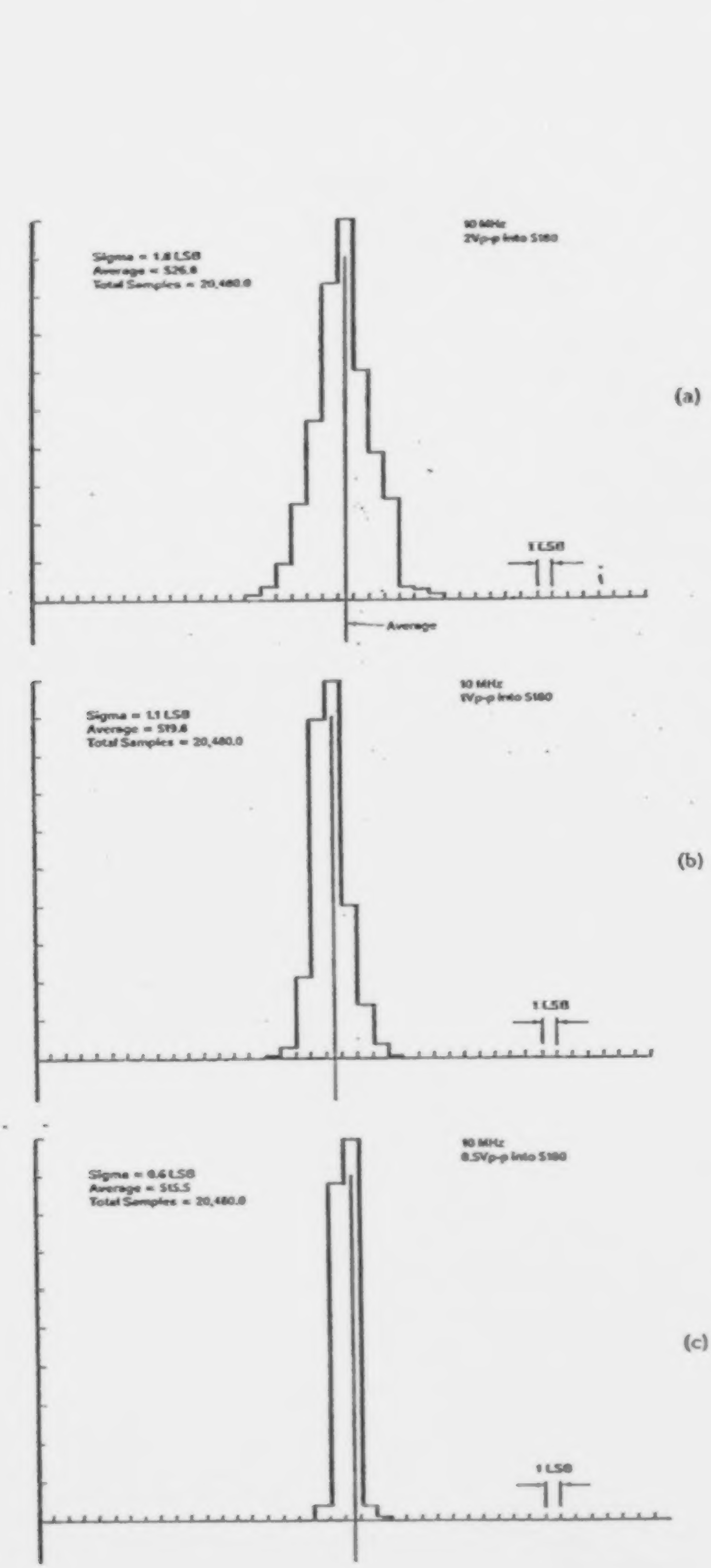


Figure 8. Locked histogram plots for the 5180A. The standard deviation from 1.8 LSB in (a) to 0.6 LSB in (c). This is due to the decrease in slew rate at the sample point. The amplitude of the 10 MHz input sinewave decreases from 2V p-p in (a) to 0.5V p-p in (c). Sampling occurred near the zero crossing in all cases. Aperture uncertainty is estimated at 35 to 50 picoseconds rms.

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is a very useful tool for evaluating A/D Converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite-time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the ADC dynamic transfer function may be measured. Figure 9 shows the test set-up for performing the FFT test. The low pass filter is used to ensure a spectrally pure sinewave. A full scale sinewave of specified frequency is input to the device under test. A 1024 point record sampled at the maximum sampling rate is then taken and input to the computer. Harmonics of the input sinewave, caused by the integral nonlinearity of the ADC, are aliased into the baseband spectrum and can be readily identified. The frequency of the input sinewave is not arbitrary and must be selected so that harmonics, aliased into baseband, do not coincide with the fundamental.

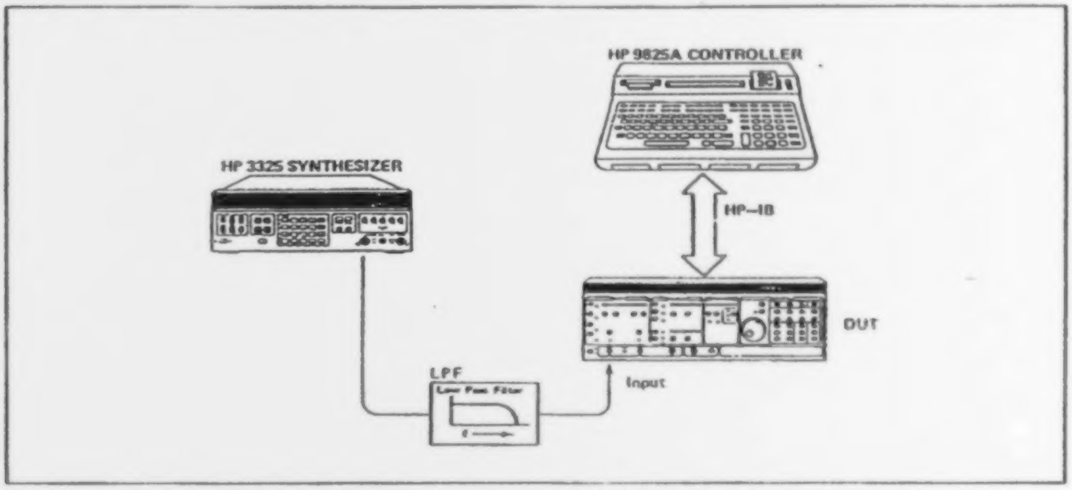


Figure 9. Test set-up for performing the Discrete Finite Fourier Transform Test.

If the ratio of the fundamental to the highest amplitude harmonic in an N bit A/D were greater than 6N dB, one could say that the error contribution of the integral nonlinearity is negligible since the amplitude of the harmonic would be smaller than the A/D's least significant bit. (Of course, even very low level harmonics can still cause encoding errors by forcing a voltage near a threshold level into an adjacent quantization band.) Figure 10 shows the graphical outputs for the 5180A for full scale sinewaves at 0.95 MHz, 4.95 MHz, and 9.85 MHz. The results for the 5180A show extremely low levels of harmonic distortion.

Figure 11 shows results of FFT testing on several waveform digitizer products. These tests were made on full scale sinewave inputs at 20 MHz sample rates. Harmonic distortion in these instances points to severe integral nonlinearity in the dynamic transfer function. Figure 12 shows the results of synthesizing an ideal N bit ADC in software and performing the FFT on the resultant idealized data. The results show the absence of harmonics of the input and likewise show the quantization noise level increasing as the number of bits in the ideal ADC is decreased. It's possible to compute signal to noise ratios from the FFT data. By summing the magnitudes of the spectral lines due to the fundamental (=S) and summing the magnitudes of the remaining spectral lines (=N), it's possible to compute 20 log S/N which is the signal to noise ratio expressed in dB. The result of doing this for the ideal ADC results in good correlation with the theoretical S/N ratio which is expressed as 6N + 1.8 dB (rms signal to rms noise).

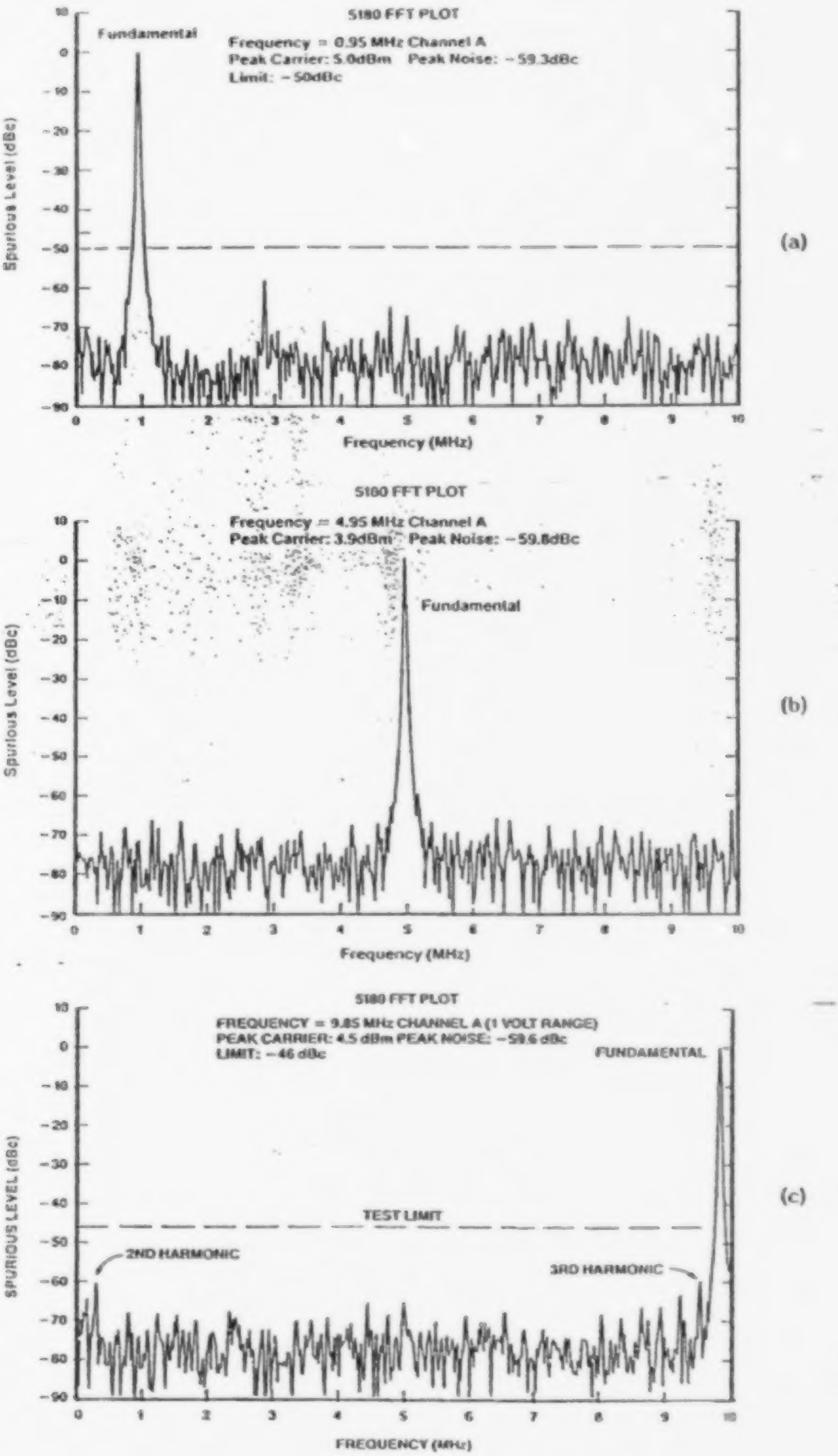


Figure 10. FFT plots on the 5180A at frequencies of 0.95 MHz (a), 4.95 MHz (b), and 9.85 MHz (c). The low harmonic distortion is indicative of a very low integral nonlinearity error.

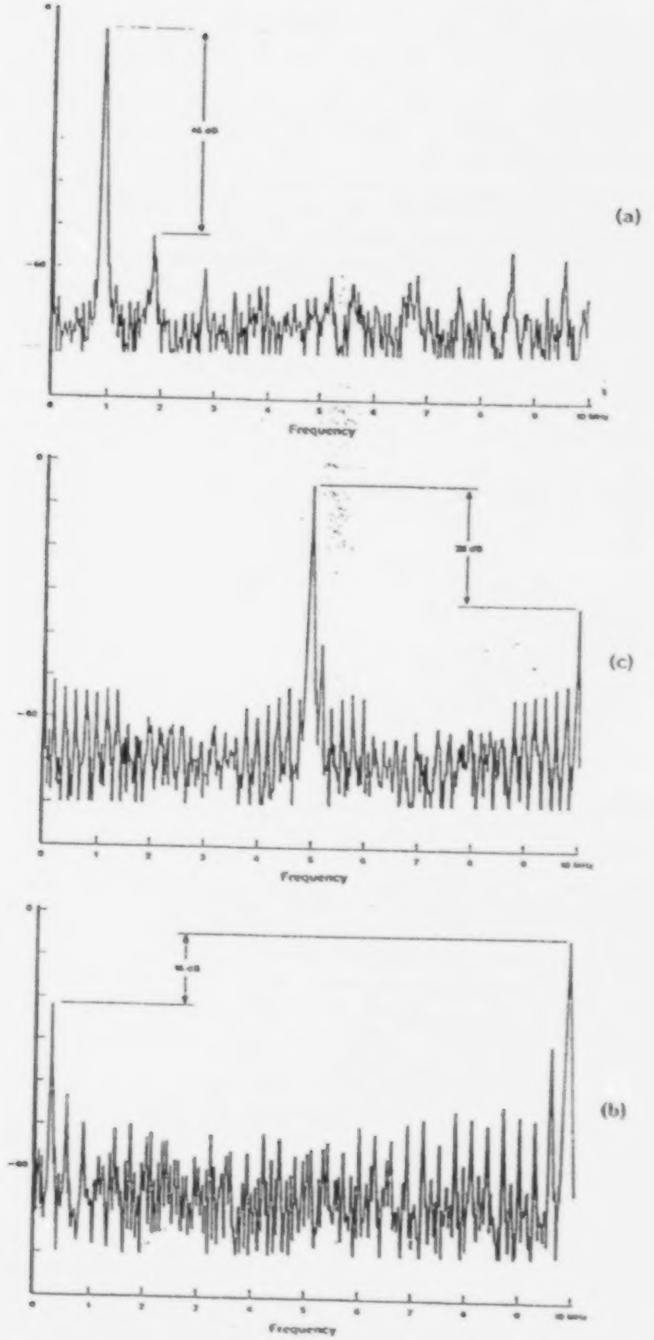


Figure 11. FFT plots for a 20 MHz, 8 bit ADC at input frequencies of 0.95 MHz (a), 4.95 MHz (b), and 9.85 MHz (c). Data at 0.95 MHz indicates low integral nonlinearity. Data at 4.95 MHz and 9.85 MHz shows the level of harmonics has increased significantly when compared to 0.95 MHz, indicating significant integral nonlinearity at higher input signal slew rates.

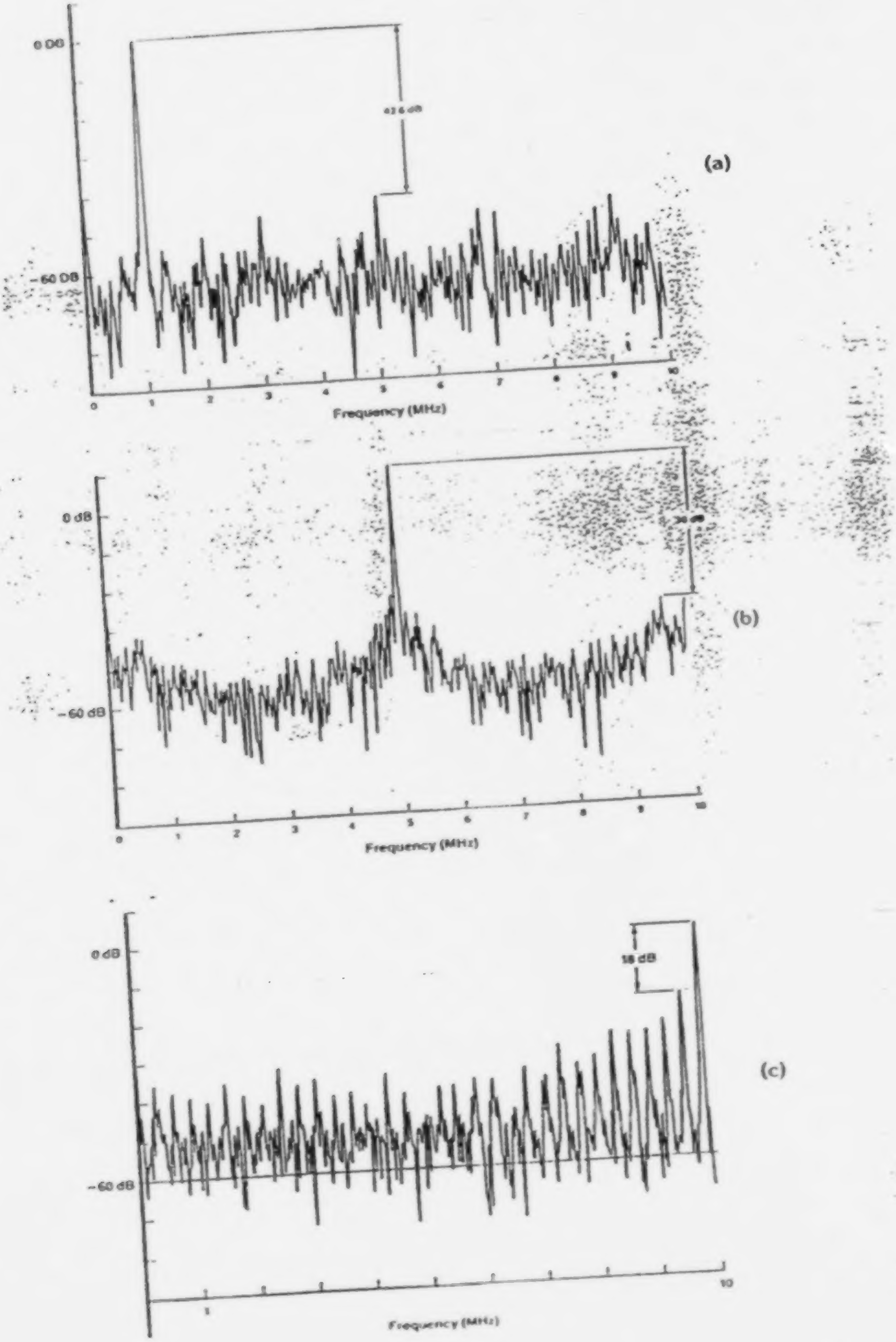


Figure 11 (cont'd). FFT plots for a 100 MHz, 8 bit ADC. Data was taken at a 20 MHz sample rate. Full scale input sinewave frequencies at 0.95 MHz (a), 4.95 MHz (b), and 9.85 MHz (c) were used. High level of harmonic distortion indicates severe integral nonlinearity.

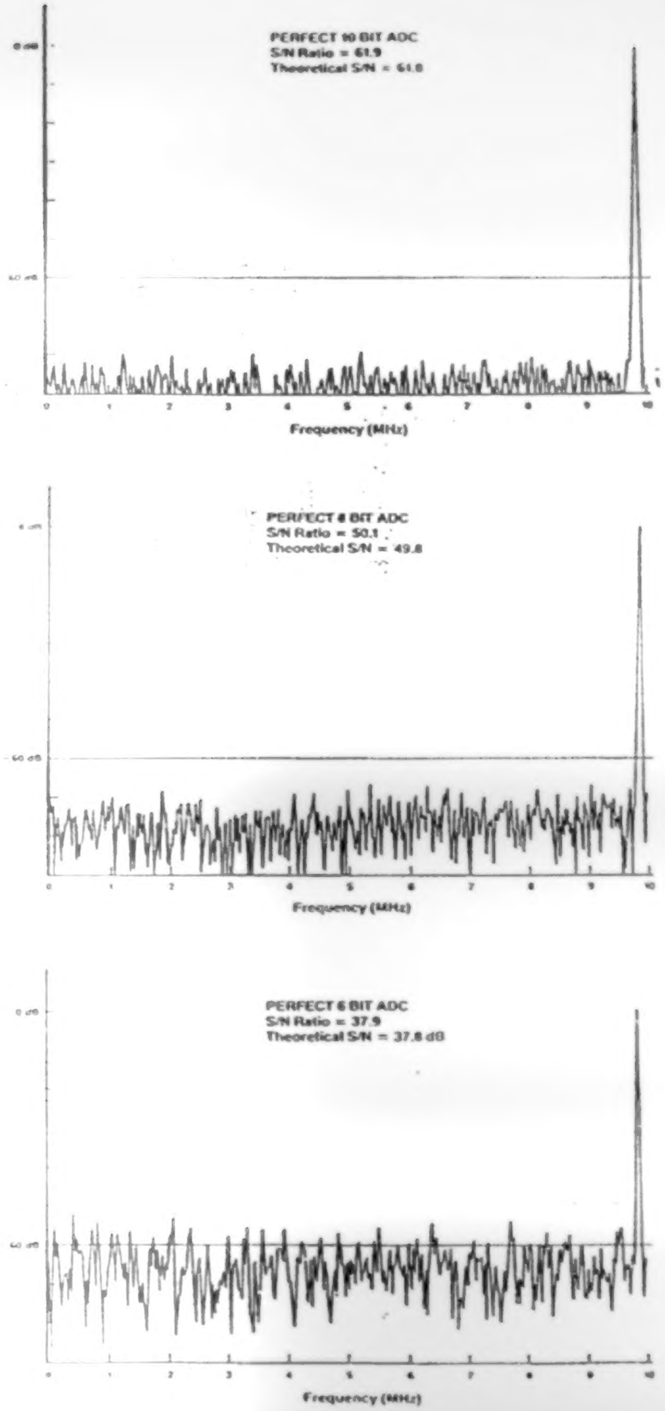


Figure 12. FFT plots on 9.85 MHz data quantized by perfect 10 bit (a), 8 bit (b), and 6 bit (c) ADC. Signal to noise ratio computed in each case agrees closely with theoretical: S/N (ideal) = 6N + 1.8 dB

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the device under test. Using least squared error minimization techniques, the software calculates an idealized sinewave fit to the data. The sinewave is of the form $A \sin(2\pi f t + \Theta) + DC$ where A, f, Θ, DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_o \sin(2\pi f_o t + \Theta_o) + DC_o$ is then ideally digitized (in software) by a perfect N bit ADC. The rms error (actual) between the actual data and the best fit sinewave is calculated. The rms error (ideal) between the idealized data (generated by the perfect N bit ADC) and the best fit sinewave is calculated. The rms error (ideal) is, therefore, the quantization error of a perfect N bit ADC. The rms error (actual) includes quantization error as well as errors due to differential nonlinearities, missing codes, integral nonlinearity, aperture uncertainty and noise.

Based upon the errors computed, an "effective number of bits" is derived. This number may be considered the number of bits in a perfect ADC whose rms quantization error would be equal to the total rms error from all sources in the ADC under test.

$$\text{effective bits} = N - \log_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}}$$

There are three important points which should be mentioned with respect to the sinewave curve fitting technique. Ignoring these points can lead to misleading (overstated) results.

1. The number of data points should be large. HP specifies that the data record contain 1024 points. Errors contributed by the ADC, if they happen to occur at the right points in the record, can change the apparent frequency of the least squared error sinewave (since frequency is one of the variable parameters) relative to the actual input frequency and thus reduce the actual RMS error. Specifying a large number of data points eliminates the possiblity that the curve fitting program would produce a sinewave whose frequency has been altered by ADC errors.
2. The test frequency should be non-harmonically related to the sample rate of the ADC in the waveform recorder. HP specifies test frequencies of 0.95 MHz and 9.85 MHz. If the input test frequency were harmonically related to the sample rate, certain codes would occur over and over again. If these codes happen to be "good" codes, then the RMS error in the record would be minimized and the effective number of bits would be overstated. By specifying non-subharmonic test frequencies, each 1024 point record will contain many different codes, thereby producing an RMS error representative of the full range of possible codes rather than a limited number of points that form a repeating pattern in the record. Non-subharmonically related test frequencies, relative to the sample rate, are essential to providing an unbiased estimate of the ADC's overall error contributions. Additionally, testing at subharmonically related frequencies can produce wide variations in the computed effective number of bits (variations of over 1 effective bit can be expected). By specifying non-subharmonically related test frequencies, test results are much more repeatable. Typically, consecutive effective number of bit computations repeat to better than 0.2 effective bits (even when the starting phase of the test record is varied between records). HP's effective number of bits specification contains a considerable amount of margin to cover this variation.

   Finally, another reason to avoid subharmonic testing is because certain harmonics are aliased back onto the fundamental, leading to a higher signal-to-noise ratio and thus a higher (but unjustified) effective number of bits.
3. The input test signal should be full scale in order to exercise the complete dynamic range and all of the codes in the ADC. HP's test for effective number of bits uses full scale sinewaves. Full scale testing is far more stringent than half-scale testing because errors due to aperture jitter, dynamic nonlinearity, noise, slewing and settling effects can all increase as the input signal level is increased to full scale. Often, the amount of degradation in ADC performance is significantly more than the ratio in amplitudes. For example, errors measured at a full scale input level are probably *more* than twice as large as the errors measured at a half scale input level. HP's full scale testing results in a conservative statement of dynamic performance.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for ADC dynamic performance and may be used to quickly judge whether or not there are any gross problems with the ADC. In this technique, a full scale sinewave input signal is offset slightly in frequency from the ADC's sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the ADC output ideally would change by 1 LSB at the point of maximum slope. Thus the ADC sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δf, is observed. Differential nonlinearities show up as horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

Figure 14 shows a beat frequency test on the 5180A. Figure 15 shows test results on several other ADC's at various full scale sinewave input frequencies.

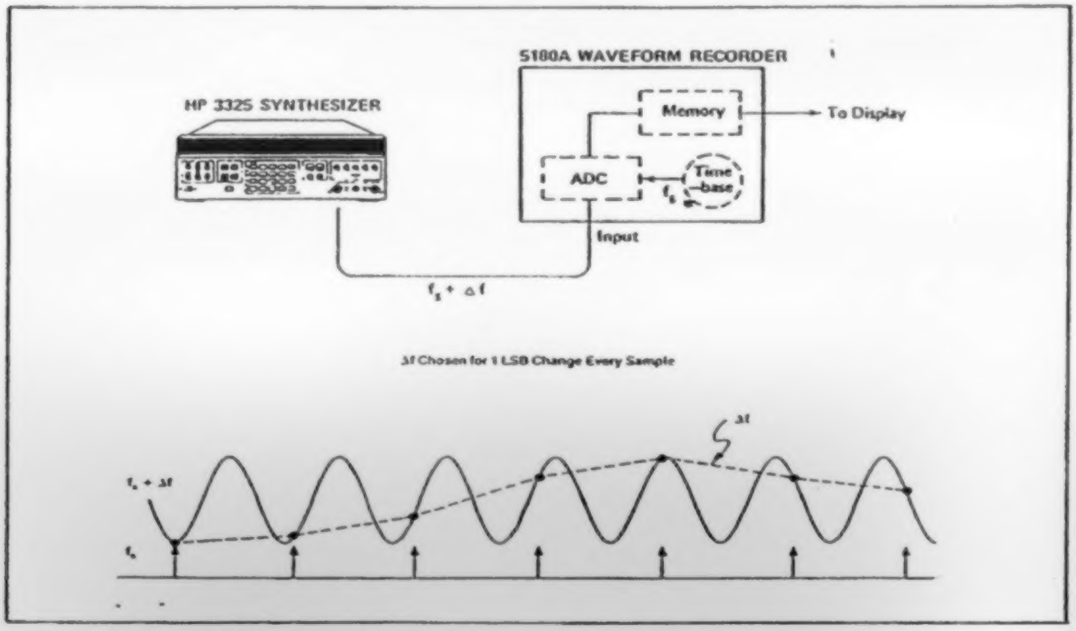
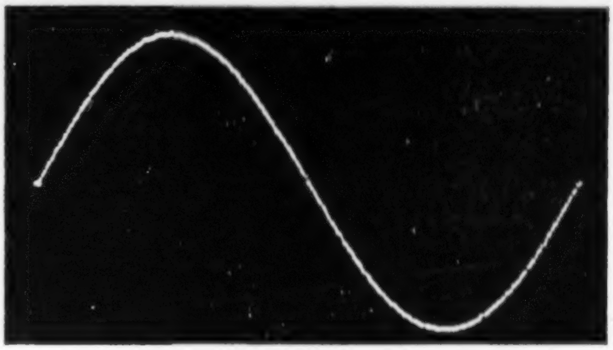
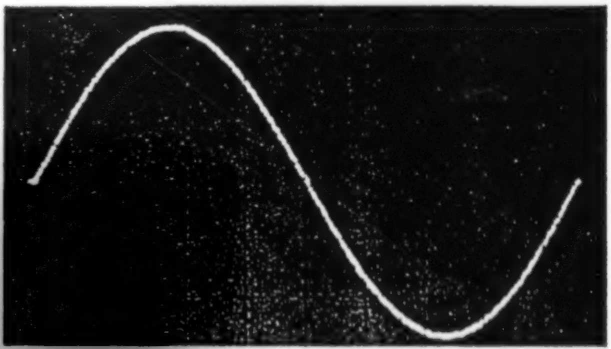


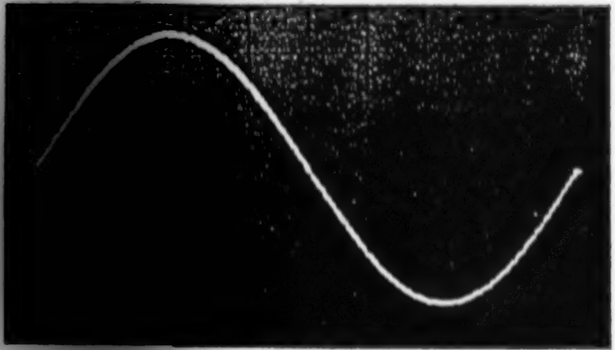
Figure 13. In the beat frequency test, the samples "walk" through the input waveform, each output code ideally changing by 1 LSB.



A— 1.00031 MHz INPUT SINEWAVE
1 μs SAMPLE INTERVAL

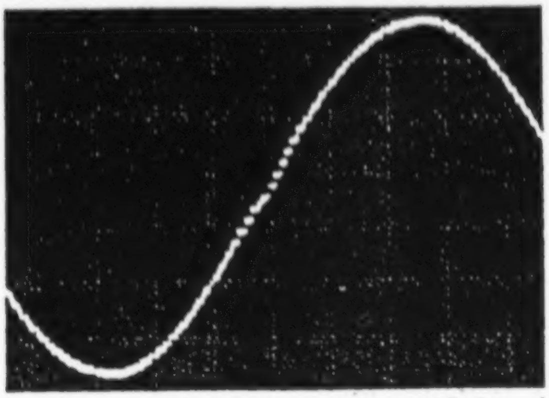


B— 5.001544 MHz INPUT SINEWAVE
200 ns SAMPLE INTERVAL

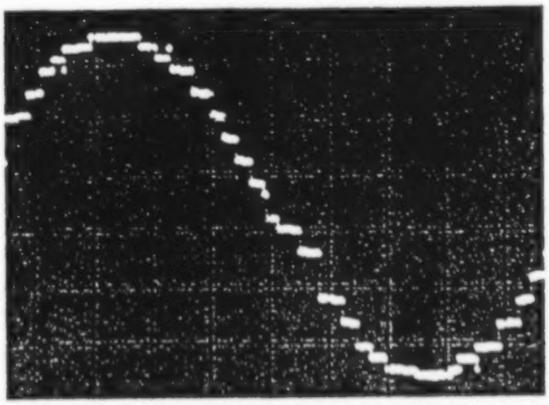


C— 10.0031 MHz INPUT SINEWAVE
100 ns SAMPLE INTERVAL

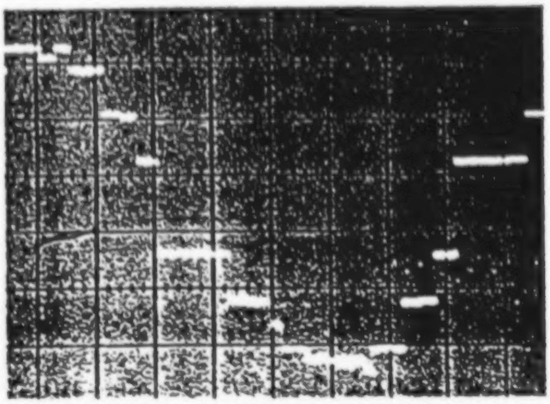
Figure 14. Beat frequency test results for 20 MHz, 10 bit ADC in the HP 5180A.



A— 1.00124 MHz INPUT SINEWAVE
1 μs SAMPLE INTERVAL

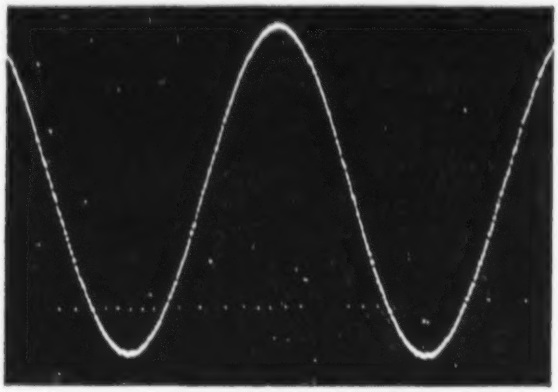


B— 5.00620 MHz INPUT SINEWAVE
200 ns SAMPLE INTERVAL

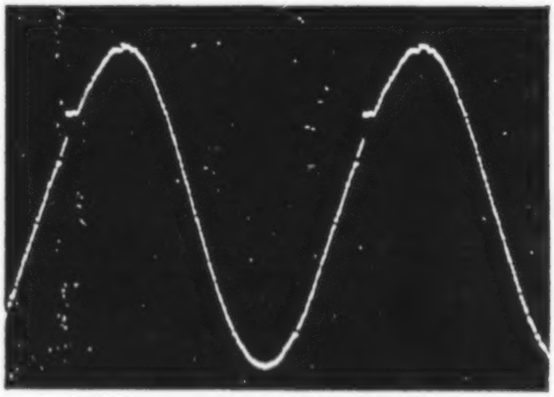


C— 10.0124 MHz INPUT SINEWAVE
100 ns SAMPLE INTERVAL

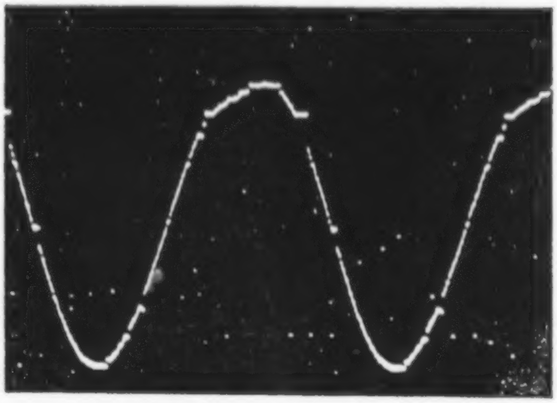
Figure 15 (cont'd). Beat frequency test results for a 100 MHz, 8 bit ADC.



A— 1.00124 MHz INPUT SINEWAVE
1 μs SAMPLE INTERVAL



B— 5.00620 MHz INPUT SINEWAVE
200 ns SAMPLE INTERVAL



C— 10.0124 MHz INPUT SINEWAVE
100 ns SAMPLE INTERVAL

Figure 15. Beat frequency test results for a 20 MHz, 8 bit ADC.

ANALOG BANDWIDTH

A factor often overlooked in evaluating an ADC for a particular application is analog bandwidth. Narrow analog bandwidth relative to the input signal bandwidth can produce amplitude error, risetime error, and when digitizing transients with rich spectral content, can produce time delay distortion due to non linear phase. Non linear phase causes a differential time delay in high frequency spectral components relative to lower frequency spectral components and thus leads to distortion in the shape of the waveform.

There are several different viewpoints concerning the input bandwidth of the ADC input channel. One viewpoint advocates narrow analog bandwidth relative to the maximum sample rate, reasoning that narrow analog bandwidth will reduce errors due to aliasing. In effect, this point of view suggests using the limited bandwidth of the ADC input as an anti-aliasing filter. The problem with this approach is that typical ADC inputs make poor anti-aliasing filters. Since the input roll off is generally controlled by a single pole, the attenuation of spectral components above fs/2 (one-half the sample rate) is generally inadequate. In addition, since the bandwidth of the ADC input is not adjustable, the anti-aliasing function, as poor as it is, is only performed at one particular sample rate. Most waveform recorders and digital storage oscilloscopes offer a multitude of sample rates spanning many decades of sample frequency. Also, the non-linear phase response of the narrow bandwidth input channel can cause significant time delay distortion in the signal seen by the ADC. And, last but not least, attenuation of in-band signals below fs/2 introduces additional amplitude errors.

Products which advocate this approach might provide a 10 MHz bandwidth ADC input for a waveform recorder with a maximum sample rate of 20 MHz. To illustrate the effects of amplitude attenuation and time delay distortion due to the ADC bandwidth, consider a full scale waveform consisting of a 2 MHz sinewave and its third harmonic at 6 MHz. With a 10 MHz analog bandwidth and assuming a single pole model, the 2 MHz signal will be attenuated to 0.98 of its original value (2% error) and will be shifted in phase by −11.31 degrees which corresponds to a time delay of 15.708 ns. The 6 MHz signal will be attenuated to 0.857 (14.3% error) and shifted in phase by −30.96 degrees, equivalent to a time delay of 14.335 ns. The differential time delay of 1.372 ns could result in an additional worst case voltage error of 2.6%, depending upon the amplitude of the 6 MHz component and slope when the signal was sampled. The total worst case measurement error is nearly 19%.

The other viewpoint advocates that the anti-aliasing function, when necessary, be performed by separate anti-aliasing filters designed specifically for that purpose. Given that anti-aliasing protection is much more effectively performed by separate filters designed for high out-of-band attenuation and linear phase, the second viewpoint advocates that the ADC bandwidth be as wide as possible. Wide ADC input bandwidth results in reduced amplitude roll off, less time delay distortion, and minimizes the interaction between the pole of the ADC input and the poles of any anti-aliasing filter used before the input. Consider the previous example using the 5180A's 40 MHz analog bandwidth. (Even better results are obtained from the wider bandwidth auxilary input.) The 2 MHz signal would be attenuated to 0.9988 of its original value (0.12%) and shifted in phase by −2.86 degrees, equal to a time delay of 3.972 ns. The 6 MHz component would be attenuated to 0.989 (1.1% error) and shifted in phase by −8.53 degrees, equivalent to a time delay of 3.949 ns. The differential time delay of 23 ps results in a worst case voltage error of only 0.04%. The total worst case measurement error would then be 1.26%, significantly less than the error for a 10 MHz bandwidth.

Measurement of analog bandwidth for waveform recorders has been difficult to do using traditional techniques, due to the ADC. However, by using a variation of the beat frequency test described earlier, this measurement is quite simple. To measure analog bandwidth with this technique, increase the input frequency until the amplitude of the displayed beat signal is 3 dB down from the low frequency full scale value. For example, Figure 18 shows test results for the 5180A's auxiliary input channel.

ENVELOPE TEST

A variation of the beat frequency test, which actually is much more demanding on the A/D converter, is the envelope test. In this test, extremes of the input signal are digitized on adjacent samples (see figure 16). With a full scale input sinewave, the positive full scale value will be digitized, followed immediately by the negative full scale value. This represents the most stringent test of settling times in the ADC. In the envelope test, a full scale sinewave at a frequency slightly offset from one-half the sampling rate is used as the input signal to the ADC. This ensures that samples will be taken on alternate half cycles of the input signal. Figure 17 shows an envelope test on the 5180A.

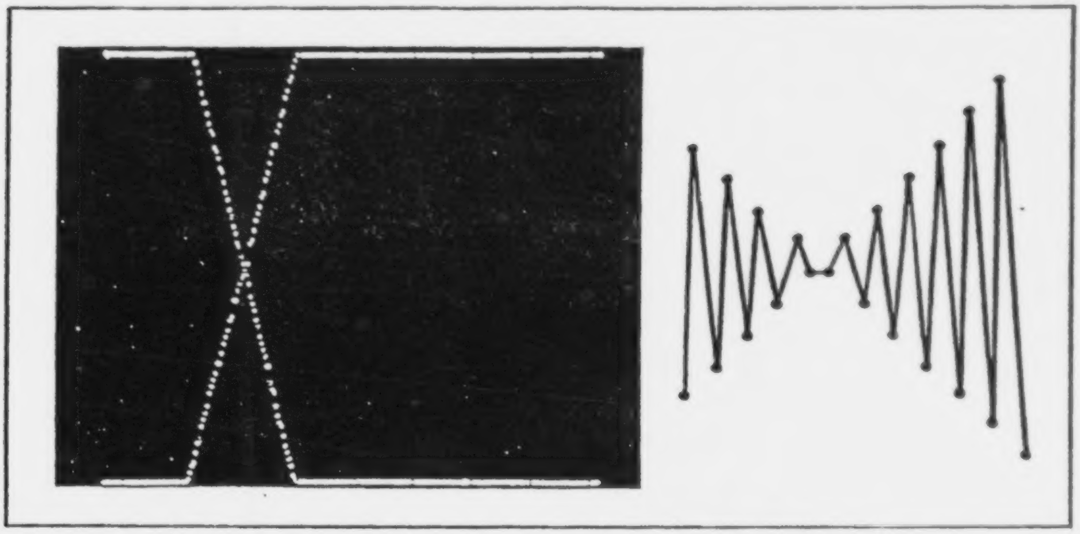


Figure 16. In the envelope test, the ADC alternates sampling on half cycles of the input sinewave.

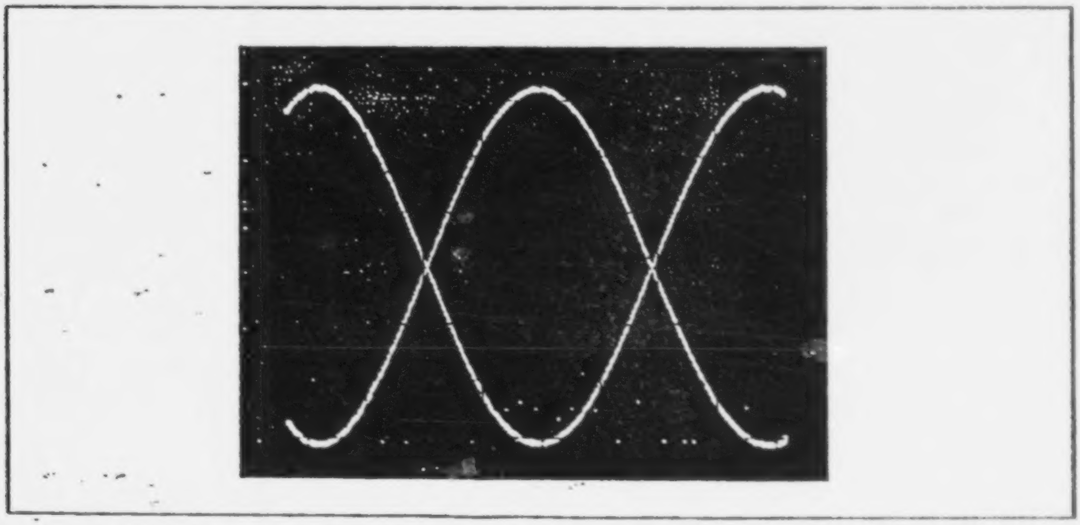


Figure 17. Envelope test on HP 5180A. Sample rate is 50 ns. Full scale input sinewave at 10.033 MHz. Even under these stringent conditions, note absence of differential nonlinearities (horizontal lines) and missed codes (gaps).

The offset frequency for a 1 LSB change on successive samples for an N bit ADC can be computed from the following (assuming a full scale input sinewave):

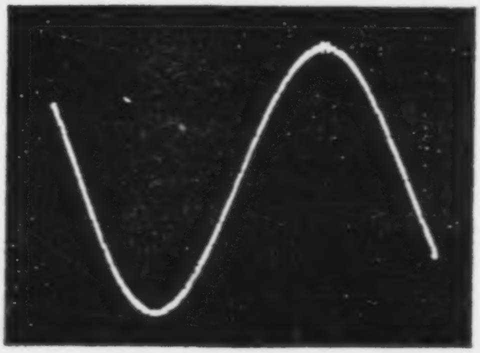
$$\Delta f = \frac{f_o}{2^N \pi}$$

Where Δf = offset frequency
f_o = waveform recorder sample rate
$f_o + \Delta f$ = synthesizer output frequency
N = number of bits in the ADC

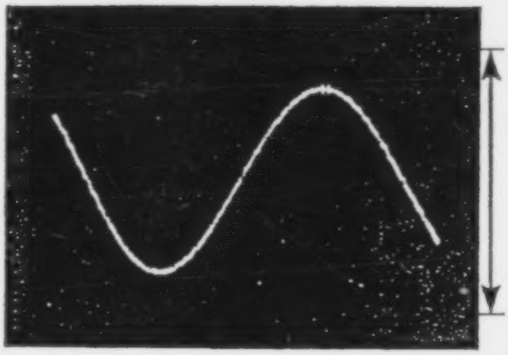
For example:

if $N = 10$ ($\Delta f = 3.11 \times 10^{-4} f_o$)

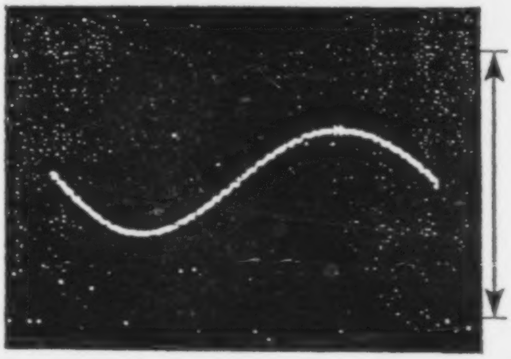
Sample rate	$f_o + \Delta f$
100 KHz	100.031 KHz
1 MHz	1.00031 MHz
5 MHz	5.00155 MHz
10 MHz	10.00311 MHz
20 MHz	20.00622 MHz



A— 1.0033 MHz
FULL SCALE SINEWAVE
6 DIVISIONS p-p



B— 100.033 MHz
FULL SCALE SINEWAVE
4 DIVISIONS p-p
(down ~ 3 dB)



C— 200.033 MHz
FULL SCALE SINEWAVE
> 2 DIVISIONS p-p

Figure 18. Amplifier bandwidth measurement for the 5180A auxiliary input channel using a beat frequency test. Bandwidth is seen to be approximately 100 MHz. Even at 200 MHz, there are remarkably few differential nonlinearities evident in the beat frequency test.

SUMMARY

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

TESTS

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes—shows up as spikes	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Missing Codes	Yes—shows up as bins with 0 counts	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Integral Nonlinearity	Yes (could be measured directly with a highly linear ramp waveform)	Yes—shows up as harmonics of fundamental aliased into baseband	Yes—part of rms error	Yes
Aperture Uncertainty	No—averaged out. Can be measured with "locked" histogram.	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Noise	No—averaged out. Can be measured with "locked" histogram.	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Bandwidth Errors	No	No	No	Yes—used to measure analog bandwidth.
Gain Errors	Yes—shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes—shows up in offset of distribution average.	No	No	No

APPENDIX I

A/D Converter Error Summary

A/D converter errors are best described by referring to the A/D's transfer function, i.e., a plot of the discrete set of output codes on the y axis versus the continuous set of input amplitudes on the x axis. Corresponding to each output code change is an input threshold level. This is usually called the quantization band edge and may be defined as the input voltage which produces two adjacent output codes, each with 50% probability. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = number of bits in the ADC.

It's important to realize that the transfer function for an A/D is very dependent upon the slew rate of the signal which it is digitizing. The transfer function for a static dc input level may appear close to the ideal (Figure 1A) while the transfer function under dynamic operating conditions may exhibit numerous errors (Figure 1B).

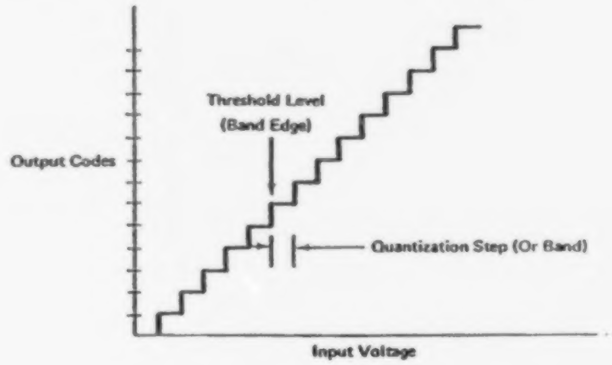


Figure 1a. Static input conditions

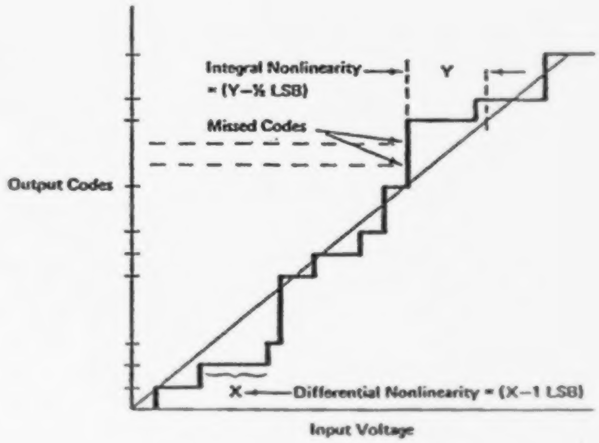

Integral Nonlinearity = (Y–½ LSB)
Y
Missed Codes
Output Codes
X
Differential Nonlinearity = (X–1 LSB)
Input Voltage

Figure 1b. Dynamic input conditions

Quantization Error

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits. A 10 bit A/D, for example, can represent an input voltage with a best case uncertainty of 1 part in 2^{10} (1 part in 1024). In real A/D's under dynamic operating conditions, the quantization band for certain codes can be significantly larger (or smaller) than the ideal. Non ideal quantization bands represent differential nonlinearity errors.

Differential Nonlinearity

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 1B shows a differential nonlinearity of 2 LSB – the actual step width is 3 LSB. The 5180A's differential nonlinearity specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be very significant.

Missing Codes

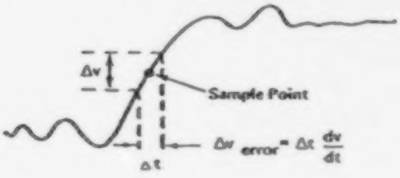
Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of −1 LSB. Figure 1B points out two missed codes in the transfer function.

Integral Nonlinearity

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line. Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 1B shows an integral nonlinearity error of 2 LSB.

Aperture Uncertainty

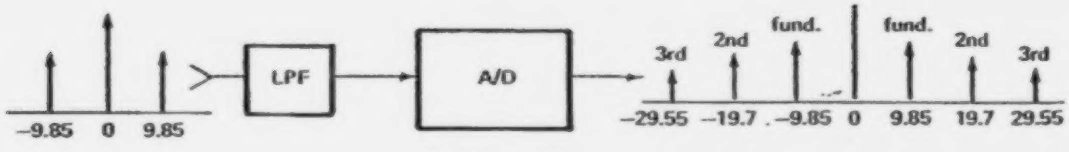
Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the ADC. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point:



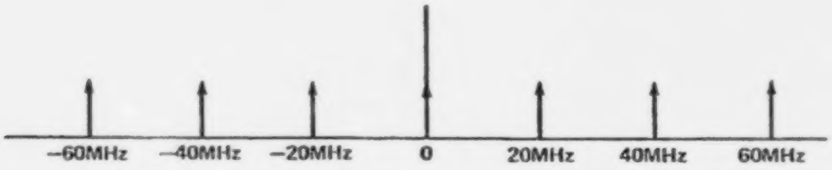
APPENDIX II

Interpreting the Frequency Domain Plot

In the DFFT test, harmonics of the input signal, produced by the nonlinearities of the A/D under test, are aliased into the baseband spectrum which is calculated by the FFT algorithm. To understand how this occurs, consider the following for the case of a 9.85 MHz input sinewave:

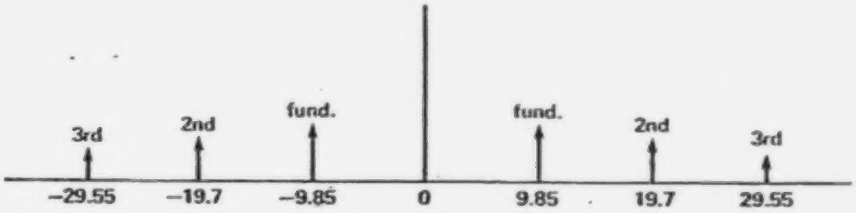


The result of sampling is to convolve the A/D output with a train of impulses separated by the sampling frequency which is 20 MHz in this case:

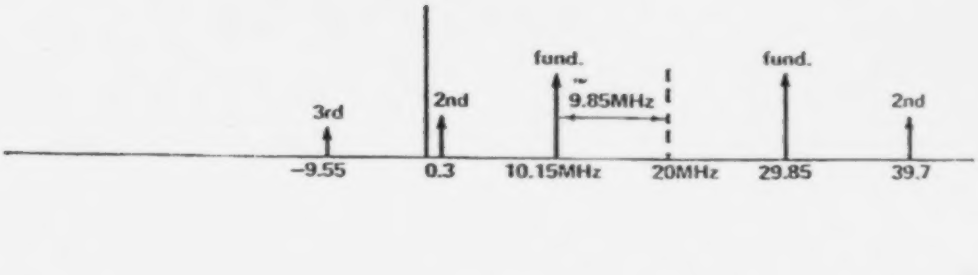


The result of this convolution is the replication of the A/D output spectrum centered about each impulse. The resultant spectrum can be considered to be the sum of the following spectra:

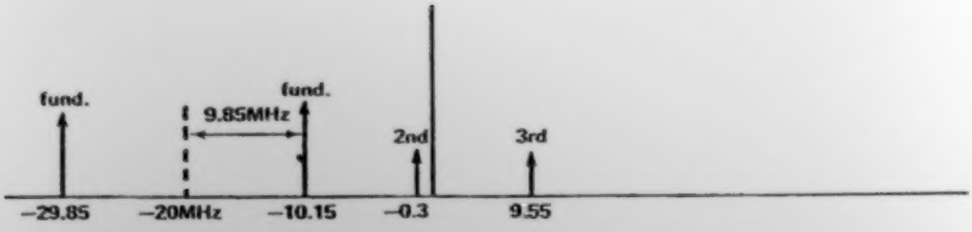
From impulse located at 0 Hz:



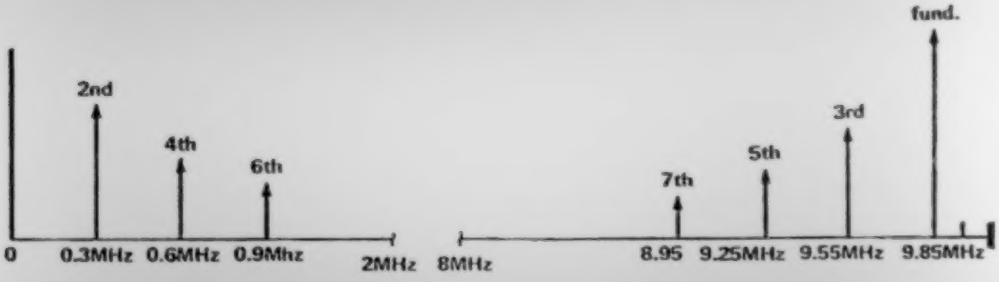
From impulse located at 20 MHz:



From impulse located at −20 MHz:



If the contributions from all the impulses are summed and if only that portion of the spectrum measured by the DFFT is examined, you see that harmonics of the fundamental show up at the following frequencies in the baseband spectrum with a separation of 300 kHz:



Particular care must be exercised in selecting the test frequency since an incorrectly chosen frequency could cause the fundamental to overlap with one of the harmonics you're trying to measure. For example, selecting 5.00 MHz would be a very poor choice of frequency since the 3rd harmonic of 5 MHz would be aliased into the baseband spectrum and show up at 5 MHz. This, of course, would mean that it would be masked by the fundamental. In testing the 5180A at a 20 MHz sampling rate, test frequencies of 0.95 MHz, 4.95 MHz, and 9.85 MHz are used.

APPENDIX III

The Discrete Finite Fourier Transform (DFFT)

The Fourier transform (forward transform) is defined as:

$$S_x(f) = \int_{-\infty}^{\infty} x(t) e^{-i2\pi ft} dt$$

$S_x(t)$ is called the Fourier transform of $x(t)$ and contains the amplitude and phase of every frequency present in $x(t)$ wihtout requiring $x(t)$ to be periodic.

For sampled data, $x(t)$ becomes $x(n\Delta t)$ where Δt is the sampling interval and n is an integer. The discrete Fourier transform is then defined as:

$$S_x^*(f) = \sum_{n=-\infty}^{\infty} x(n\Delta t) e^{-i2\pi fn\Delta t} \Delta t$$

However, this transform no longer contains accurate amplitude and phase information for all frequencies present in $x(t)$. Rather, $S_x^*(f)$ accurately describes the spectrum of $x(t)$ up to a maximum frequency, F_{MAX}, which is equal to $1/(2\Delta t)$. There is one problem with $S_x^*(f)$ – you need to take an infinite number of samples.

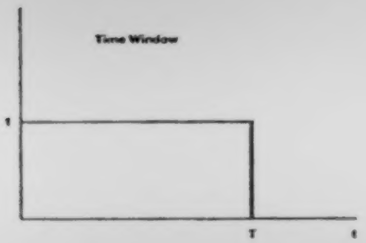
The finite discrete Fourier transform limits the observation of $x(t)$ to a finite time window, T, where $T = N\Delta t$ and N = total number of samples in the record. The discrete finite Fourier transform is defined as:

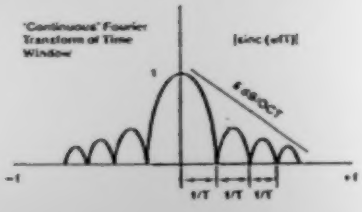
$$S_x^*(f) = \sum_{n=0}^{N-1} x(n\Delta t) e^{-i2\pi m\Delta f\, n\Delta t} \Delta t$$

Since there are only a finite number of time data points, the DFFT produces a finite number of frequency points, $m\Delta f$, where amplitude and phase of the spectrum of $x(t)$ can be calculated. The discrete frequency points, Δf, are spaced every $1/T$ apart. Thus N data points in the time domain produce $N/2$ complex quantities (amplitude and phase) in the frequency domain.

Windowing

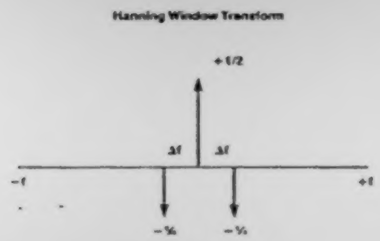
Truncating the sampled time domain waveform to a finite number of data points is the same as multiplying the waveform by a rectangular window. Multiplication in the time domain is analagous to convolution of the corresponding transforms in the frequency domain.

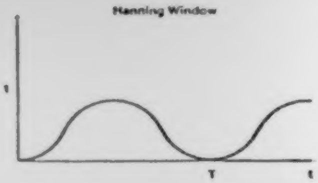




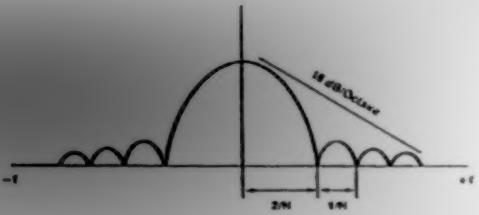
Convolving the spectrum of $x(n\Delta t)$ with a sinc function "smears" the calculated spectrum of $x(t)$ because of "leaks" of the spectral amplitudes of $Sx(f)$ through the sidelobes of the sinc function.

If the time window is modified, the leakage effects via the side lobes can be reduced. The Hanning function, defined as: $\left|\frac{1}{2}-\frac{1}{2}\cos\frac{(2\pi t)}{T}\right|$, greatly reduces the side lobe amplitudes.





The result of the convolution of the two window functions (the sinc function convolved with the transform of the Hanning window) is:



You see that the main lobe of the modified window function is widened and flattened, while the side lobes are greatly reduced in amplitude. In the FFT algorithm used to implement the DFFT for the 5180A test, the time domain data is modified by the Hanning window.

APPENDIX IV

Dynamic Performance Test Software

Introduction

This appendix includes the system set-up, annotated program listings, and measurement considerations for the histogram, FFT, and sine wave curvefit tests. The histogram program calculates and plots differential nonlinearity for the ADC under test. The number of missing codes is also calculated. The FFT test and resulting plot show maximum spurious signal level in dB below the carrier. The number of effective bits and S/N ratio are calculated in the sine wave curvefit test.

Although the software is written specifically for the HP5180A, variables such as number of bits and sampling rate can be changed to allow the testing of other digitizers. A list of program lines which need to be changed is explained under software revisions.

Equipment Set-Up

The equipment set-up for an A channel FFT test at 0.95 MHz is shown in figure 1. For the sine wave curvefit test the plotter is not needed, as test results are listed on the 9825 B/S printer. The histogram set-up is the same as figure 1, except that the filter is not used.

Filter assembly, 10871-60002, contains three low-pass filters at 1, 5, and 10 MHz. Required for the FFT and sinewave curvefit tests, the filter prevents harmonics of the input sinewave from being shifted or aliased into the baseband. At twice the cut-off frequency, the input signal is attenuated by at least 60 dB.

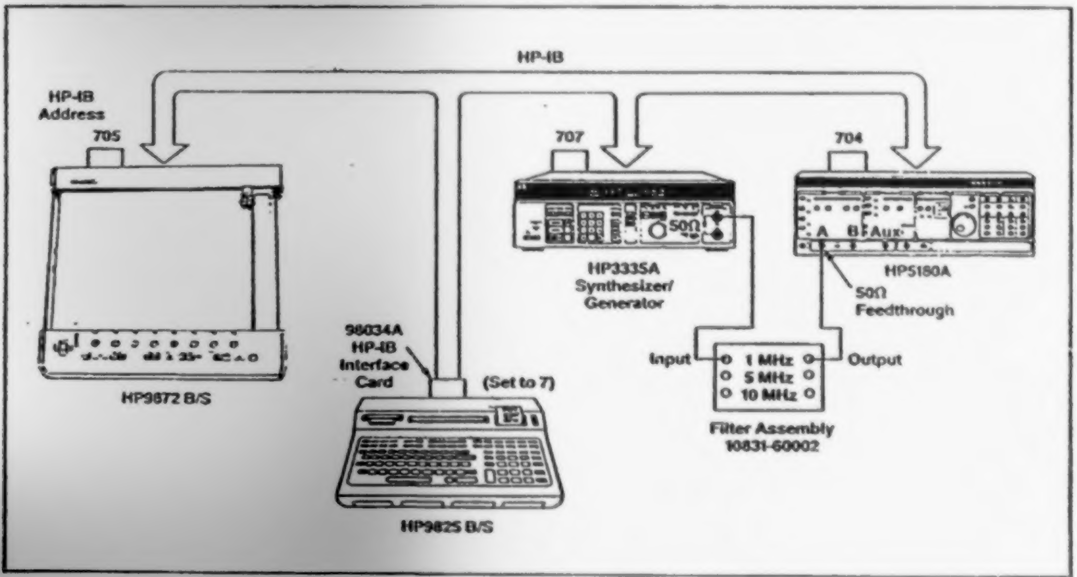


Figure 1. FFT Channel A, 0.95 MHz Set-up

Equipment Description

Table 1 includes a list and description of required test equipment. A 50Ω feedthrough is required for any A or B channel measurement.

Table 1. Required Equipment

HP Part No.	Description
5180A	Waveform Recorder
9872 B/C	Graphics Plotter
10831-60002	1, 5, 10 MHz Filter Assembly
3335A	Synthesizer/Generator
9825 B/S	Computing controller includes String/Advanced programming, Plotter, General I/O, Extended I/O ROMS, and 22K bytes user memory
98034A	HP-IB interface card
10100C	50Ω feedthrough

Critical specifications for the selection of the HP3335A as the signal source include absolute accuracy (±0.2 dB), harmonic distortion (−40 dBc, >2 MHz), spurious noise (−75 dBc), and phase noise (−60 dB). Phase noise is important when analyzing sine wave curvefit data. Accurate amplitude settability is required by the histogram test.

Measurement Considerations

Test Frequencies

Test frequencies harmonically related to the waveform recorder sampling rate can not be used. 0.95 MHz and 9.85 MHz, are used to test the HP5180A as they are not coherent with its 20 MHz sampling rate.

Test Amplitude

For the histogram, the amplitude of the input sinewave must be at least full-scale, preferably slightly greater than full scale. A 2.2V peak-to-peak amplitude is used to test the 5180A (full-scale equal to −1.024V/+1.022V)

The sine wave curvefit and FFT input signal amplitudes may be equal to or less than full-scale, but invalidate the measurement calculation if greater than full-scale range.

Histogram

At least 20,000 samples of data should be used to insure measurement repeatability.

Amplitude of the sinewave at the input to the ADC must be known accurately for use in the differential nonlinearity calculation. The calculation also assumes no dc offset in the input signal or A/D converter.

Roll-off due to limited input bandwidth may attenuate the input signal measured by the ADC under test. In this case, the amplitude used to program the synthesizer and in the differential nonlinearity calculation would be greater than the actual amplitude into the ADC under test. This would result in a differential nonlinearity calculation which is undercorrected. The plot would slightly resemble the probability density cusp of a sinewave instead of being linear. If the actual amplitude into the ADC is greater than the peak voltage variable in the differential nonlinearity calculation, the plot will be overcorrected or "bowed down". The 5180A program assumes no roll-off, since the input bandwidths are greater than 40 MHz.

Sine Wave Curvefit

A phase guess of the input sinewave within thirty degrees is important, as it insures iterating to the correct value. The phase guess software included provides an even closer guess of the phase, requiring less iterations and significantly less test time. For the 5180A test frequencies and sampling rate used, the initial phase guess is typically within one tenth of a degree, requiring less than three iterations.

FFT

Due to calculator user memory of 22K bytes, the maximum number of data points is 2048. In the HP5180A performance test, one record of 1024 data points is used.

Software Adaptations

To adapt the software for an ADC other than the HP5180A, ADC setup and data I/O commands need to be revised. Some measurement variables such as number of bits and sampling rate may also need to be changed. Program lines affected by these changes are listed in table 2 for each of the tests.

Offset binary is the data format used in all programs. A simple driver program to convert to offset binary coding would be required for data in other formats.

Table 2. Program line numbers to be revised

	Histogram	FFT	Sine wave curvefit
Variable selection	18:19	16:17	17:18
ADC set-up	34:36	33:35	33:35
Data collection	38:50	37:45	37:44

Line 19 in the histogram test initializes the number of bits, the full-scale range, the sampling rate of the ADC, and the amplitude of the synthesizer. The number of data points in one record and the number of records is also set.

In the FFT test line 17 initializes the number of data points, and sampling rate of the ADC as well as the amplitude of the synthesizer.

In the sine wave curvefit test, sampling rate, number of bits, and full-scale range of the ADC is set in line 18. The maximum number of iterations may also be changed if desired.

For all tests if the ADC front panel settings can not be programmed by HP-IB, the measurement can be set up manually and triggered. In this case, the ADC set-up routine would be deleted, although the data collection subroutine still would need to be revised.

*5180A set-up:

Preset, record length, sample rate, channel, A and B channel range to 1V (− 1.024, + 1.022 full scale), trigger position to zero seconds, and external trigger

```
0: "Start histogram":
1:
2: "Variable explanation":
3: "A is amplitude(dBm)":
4: "C is 5180A input channel":
5: "F is sinewave input frequency":
6: "M is the number of missing codes":
7: "N is the number of bits(10 for 5180A)":
8: "P is the peak voltage(calculated from A)":
9: "R is the number of records":
10: "S is the sampling interval(sec/sample)":
11: "V is full scale range":
12: "X is the number of data points in one record":
13: "X[2↑N] is the histogram data array":
14: "D[2↑N]is the calculated differential nonlinearity array":
15:
16: "Initialize":
17: dev "5180",704,"3335",707 ———— HP-IB select codes of ADC and synthesizer
18: dim X[1024],D[1024];csv ———— dimension variables
19: 10→N;1024→X;20→R;2.046→V;11→A;5e-8→S —— set number of bits, number of data points in one record, number
20:                                            of records, full scale range, amplitude (dBm), and sampling rate
21: "FREQUENCY":          }
22: ent "FREQ(MHz)?",F    } ———— enter a frequency non-coherent with the sampling rate
23:                              (0.95 and 9.85 MHz test frequencies used for 5180A)
24: "Amplitude(dBm→peak volts)":  }
25: √2*√(.05*10↑(A/10))→P         } ———— peak amplitude in volts calculated from dBm, for
26:                                      use in differential nonlinearity calculation
27: "Channel Select":                  }
28: ent "Channel?(A=1,B=2,AUX=4)",C    } ———— select ADC input channel
29:
30: "Set-up synthesizer":                 }
31: fmt 1,"F",f.2,"M,A",f.2,"K"           } ———— frequency and amplitude commands sent to synthesizer
32: wrt "3335.1",F,A                      }
33:
34: "Set-up ADC":                                                        }
35: fmt 2,"pr,le",f,",","mm",e,",","ch",f.0,"arl,brl,sal,pt0,sel"    } 5180A
36: wrt "5180.2",X,S,C                                                   } set-up
37:
38: "Data collection":
39: for L=1 to R ———— loop for number of data records
40: fxd 0;dsp "data record",L
41: wrt "5180","sa4" ———— arm HP5180A
42: if bit("10xxx",rds("5180"));gto +0 ———— check 5180A status for arm command received
43: wait 10;wrt 704,"mt" ———— trigger HP5180A
44: if bit("0xx",rds("5180"));gto +0 ———— check 5180A status for measurement complete
45: wrt "5180","obl" ———— command sent to output data
46: for I=1 to X ———— loop for number of sample points per record
47: red "5180",B;B+1→B    }
48: X[B]+1→X[B]           } ———— histogram bin corresponding to the voltage read
                                  from the ADC is incremented
49: next I
50: next L
51:
52: "Differential nonlinearity":
53: rad;for I=2 to 2↑N-1
```

```
54: X[I]/RX→D[I]                                              actual hits divided by total samples
55: D[I]/((asn(V(I-2↑(N-1))/(P*2↑N))                          given sinewave probability density function
      -asn(V(I-1-2↑(N-1))/(P*2↑N)))/π)→D[I]                   actual probability of hits is calculated
56: D[I]-1→D[I]                                    ideal stepwidth (1 LSB) is subtracted from actual step size
57: dsp "diff nonlinearity",I                          to determine differential nonlinearity for each code
58: next I
59: 0→D[1]→D[2↑N]
60:
61: "calculate missing codes":
62: for I=1 to 2↑N
63: if X[I]=0;M+1→M                                               number of missing codes calculated
64: next I
65:
66: ent "plot diff nonlinearity?(yes=1)",J
67: if J#1;gto "end"
68:
69: "Differential Nonlinearity Plot":
70: dsp "plot non-linearity"
71: psc 705                                                                     plotter select code
72: scl -2↑N/6,2↑N+2↑N/12,-3,N+1
73: csiz
74: pen# 1
75: for I=1 to 2↑N
76: plt I-1,D[I]                                               differential nonlinearity data is plotted
77: next I
78: pen# 2
79: fxd 0;xax -1,64,0,2↑N,4                                                              axes plotted
80: fxd 1;yax 0,.25,-1,N-3,4
81: plt 2↑N/2.5,-2.5,1
82: lbl "ADC CODE"
83: deg;csiz 1.5,2,1,90
84: plt -2↑N/6+2↑N/12,.5,1
85: lbl "Non-linearity in LSB"                                                         labels plotted
86: plt 0,N-.5,1
87: csiz 3;lbl "5180A HISTOGRAM TEST"
88: cplt ;csiz 2
89: lbl "DIFFERENTIAL NON-LINEARITY PLOT"
90: cplt ;csiz 1.5
91: fxd 2;lbl "Input Level=",2P,"Vp-p "
92: lbl "Frequency=",F,"MHz"                                  input signal level, frequency,
93: cplt ;fxd 0                                           and number of missed codes plotted
94: lbl "Total samples=",RX," #Missed Codes=",M
95: pen# 0                                                                     plotter pen lifted
96:
97: "end":end
*32068
```

```
0: "Start sinewave curvefit":
1:
2: "Variable explanation":
3: "C is 5180 input channel":
4: "E is the RMS error":
5: "F is sinewave input frequency":
6: "K is the total number of samples":
7: "L is the maximum number of iterations":
8: "N is the number of bits(10 for 5180A)":
9: "P is the phase":
10: "S is the 5180 sample interval(seconds/sample)":
11: "V is the full scale range":
12: "W is amplitude(dBm)":
13: "X[K] is actual data array dimensioned to K points":
14:
15: "Initialize":
16: dev "5180",704,"3335",707 ———————— HP-IB select code of ADC and synthesizer
17: dim X[1024] ———————————————————————— dimension variable
18: csv;5e-8→S;1024→K;10→L;10→N;2.046→V ——— set sampling rate, number of samples, maximum number
                                              of iterations, number of bits, and full-scale range
19:
20: "Frequency":             }
21: ent "FREQ(MHz)?",F       } ——— enter a frequency non-coherent with the sample rate
                                   (0.95 and 9.85 MHz test frequencies used for 5180A)
22:
23: "Amplitude":             }
24: ent "Amplitude(dBm)?",W  } ——— Enter amplitude in dBm (≤ 1 full-scale range)
25:
26: "Channel select":                }
27: ent "Channel(A=1,B=2,AUX=4)?",C  } ——— select ADC input channel
28:
29: "Set-up synthesizer":                }
30: fmt 1,"F",f.2,"M,A",f.2,"K"          } ——— frequency and amplitude commands sent to synthesizer
31: wrt "3335.1",F,W                     }
32:
33: "Set-up ADC":                                                          }
34: fmt 2,"pr,le",f,",","mm",e,",","ch",f.0,"arl,brl,sal,pt0,sel"          } 5180A set-up"
35: wrt "5180.2",K,S,C                                                     }
36:
37: "Data collection":
38: wrt "5180","sa4" ——————————————————————— arm HP5180A
39: if bit("10xxx",rds("5180"));gto +0 ———— check 5180A status for arm command received
40: wrt 704,"mt" ——————————————————————————— trigger HP5180A
41: if bit("0xx",rds("5180"));gto +0 —————— check 5180A status for measurement complete
42: wrt "5180","obl" ——————————————————————— command sent to output data
43: dsp "collecting data"
44: for I=1 to K;red "5180",X[I];next I ——— K samples are read into data array
45:
46: "Phase Guess":                                                      }
47: 0→r47→r48→r49                                                       }
48: acs(2((X[1]-min(X[*]))/(max(X[*])-min(X[*])))-1)→G                  }
49: 2(X[2]-min(X[*]))/(max(X[*])-min(X[*]))-1→r47                       } ——— phase guess of data made
50: abs(cos(G+360SF)-r47)→r48                                           }
51: abs(cos(360-G+360SF)-r47)→r49                                       }
52: if r49<r48;-G→G                                                     }
53:
```

```
54: "Curvefit":
55: deg;F*1e6→F ———————————————————— frequency converted from MHz to Hz
56: for J=1 to L —————————————————————————————— iteration loop
57: 0→r1→r2→r3→r4→r5→r6→r7→r8→r9→r10→r11→r12→r13→r14→r15→r28
58: for I=1 to K
59: fxd 0;dsp "Iteration #",J,I/K*100,"% DONE"
60: (I-1)S→T;360FT+G→X;cos(X)→A;sin(X)→B
61: AA+r1→r1;BB+r2→r2;AB+r3→r3;ABT+r4→r4;BBT+r5→r5;BBTT+r6→r6
62: AX[I]+r7→r7;BX[I]+r8→r8;BTX[I]+r9→r9;A+r10→r10;X[I]↑2+r28→r28
63: B+r11→r11;X[I]+r12→r12;BT+r13→r13;AT+r14→r14;BTT+r15→r15
64: next I
65: r10/K→r10;r11/K→r11;r12/K→r12
66: r1-r10r10K→r16;r4-r10r13→r17;r5-r11r13→r18
67: r3-r10r11K→r19;r3-r11r10K→r20;r4-r11r14→r21             iteration
68: r6-r11r15→r22;r2-r11r11K→r23;r7-r12r10K→r24              algorithm
69: r8-r12r11K→r25;r9-r12r13→r26
70: r26/r24-r17/r16→R;r25/r24-r19/r16→D
71: (r17r21-r16r22)/r16r16→U;(r17r20-r16r18)/r16r16→P
72: (r19r21-r16r18)/r16r16→Y;(r19r20-r16r23)/r16r16→Z
73: F+(ZR-PD)/2π(UZ-PY)→F;(UD-YR)/π(UZ-PY)*180→r27
74: if abs(r27)>10;r27/ln(abs(r27))→r27
75: G+r27→G;(G+180)mod360-180→G
76: (r24+r25+r26)/(r16+r19+r17)→M;r12-Mr10→H
77: √((r28+MMr1-2Mr7)/K+HH-2H(r12-Mr10))→E
78: beep
79: fxd 0;prt "#",J ——————————————————————————— iteration number
80: fxd 2;prt "F",F ——————————————————————————— frequency guess
81: prt "P",G ———————————————————————————————— phase guess
82: prt "M",100M/2↑(N-1),"%" ————————————— peak magnitude (% of full-scale)
83: prt "H",(H-2↑(N-1))V/2↑N ——————————————————————— DC offset
84: prt "RMS",E;spc ————————————————————————————— RMS error
85: if abs(G-r30)<.0001;gto "Calculation" ——— if difference in phase for two successive iterations
86: G→r30                                     is less than .0001, rms error is at a minimum; branch
87: next J                                     to calculate effective bits and S/N ratio
88: fxd 0;prt "Did not converge in",L,"iterations"
89: gto "end"
90:
91: "Calculation":
92: dsp "calculating"
93: fxd 1;N-log(E*√12)/log(2)→r33;prt "EFF.BITS=",r33 ———— calculate effective bits
94: prt "S/N RATIO=",6r33+1.8;spc 2 ————————————————— calculate S/N ratio
95:
96: "end":end
*10033
```

```
0: "Start FFT":
1: "Variable explanation":
2: "A is amplitude in dBm":
3: "C is 5180 input channel":
4: "F is the sinewave input frequency":
5: "G is peak noise level":
6: "M is carrier signal level":
7: "2N is equal to the block size or # of data points":
8: "R is sampling rate(MHz)":
9: "S is sampling interval(time/sample)":
10: "C[N/4+3] is a reference array dimensioned to N/4+3":
11: "I[12] is an array dimensioned to 12":
12: "X[N],Y[N] are data arrays dimentioned to N":
13:
14: "Initalize":
15: dev "5180",704,"3335",707 ——— HP-IB select codes of ADC and synthesizer
16: dim X[512],Y[512],C[131],I[12] ——— dimension variables
17: 512→N;11→W;20→R;1/(R*1e6)→S ——— set number of data points, amplitude,
18:                                    sampling rate (MHz and seconds/sample)
19: "FREQ":                } ——— enter a frequency non-coherent with the sampling rate
20: ent "FREQ,(MHz)?",F    }     (0.95 and 9.85 MHz test frequencies used for 5180A)
21:
22: "Amplitude":ent "Amplitude(dBm)?",A ——— enter amplitude in dBm (≤ full-scale)
23:
24: "Channel select":                    } ——— select ADC input channel
25: ent "Channel?(A=1,B=2,AUX=4)",C      }
26:
27: "Filter":dsp "Filter connected to input?";stp
28:
29: "Set-up synthesizer":                } 
30: fmt 1,"F",f.2,"M,A",f.2,"K"          } ——— frequency and amplitude commands sent to synthesizer
31: wrt "3335.1",F,A                     }
32:
33: "Set-up ADC":                                                          } 5180A
34: fmt 2,"pr,le",f,",","mm",e,",","ch",f.0,"arl,brl,sal,pt0,sel"      } set-up
35: wrt "5180.2",2N,S,C                                                    }
36:
37: "Data collection":
38: wrt "5180","sa4" ——— arm HP5180A
39: if bit("10xxx",rds("5180"));gto +0 ——— check 5180A status for arm command received
40: wait 10;wrt "5180","mt" ——— trigger HP5180A
41: if bit("0xx",rds("5180"));gto +0 ——— check 5180A status for measurement complete
42: wrt "5180","obl" ——— command sent to output data
43: dsp "collecting data"
44: for I=1 to N;red "5180",X[I];next I ——— read N points into X data array
45: for I=1 to N;red "5180",Y[I];next I ——— read N points into Y data array
46:
47: "Fill":deg                                   }
48: 360/N→r2;N/4+1→r3                            } ——— quarter-cycle of a sinewave
49: for I=1 to r3;sin(r2(I-1))→C[I];next I       }     stored in C array for use in FFT
50: sin(r2/2)→C[r3+1];cos(r2/2)→C[r3+2]         }
51:
```

```
52: "Hanning":dsp "Hanning"
53: for I=1 to N;(X[I]-N)(1-cos(360I/(2*N)))/(N/4)→X[I];
      next I
54: for I=1 to N;(Y[I]-N)(1-cos(360(I+N)/(2*N)))/(N/4)→Y[I]
55: next I
56:
57: "FFT calculation":
58: dsp "COMPUTING FFT"
59:
60: "lace":
61: N-1→r3;N+r3→r4
62: for J=1 to r3 by 2;1→r5;J→I[1]
63: if flg1;gto "end"
64: 2I[r5]→I[r5+1]
65: if I[r5+1]>r4;I[r5+1]-r4→I[r5+1]
66: if I[r5+1]<I[1];gto "lce"
67: if I[r5+1]#I[1];r5+1→r5;gto -3
68: r5→r6;1→r7
69: if I[r6]<=r3;gto +2
70: Y[I[r6]-r3]→r8;gto +2
71: X[I[r6]+1]→r8
72: for I=r6 to r7 by -1
73: I-1→r9;if r9=0;r5→r9
74: if I[r9]<=r3;gto +2
75: Y[I[r9]-r3]→r10;r8→Y[I[r9]-r3];gto +2
76: X[I[r9]+1]→r10;r8→X[I[r9]+1]
77: r10→r8;next I
78:
79: "lce":next J
80:
81: "bfft":int(ln(N)/ln(2)+.5)→r3;N/2→r4;N/4→r5
82: 1→J;for I=1 to N-1
83: if I>=J;gto +3
84: X[J]→r7;Y[J]→r8;X[I]→X[J];Y[I]→Y[J]
85: r7→X[I];r8→Y[I]
86: r4→r9
87: if r9>=J;gto +2
88: J-r9→J;r9/2→r9;gto -1
89: J+r9→J;next I
90: for L=1 to r3
91: if flg1;gto "end"
92: 2↑L→r10;r10/2→r11
93: for J=1 to r11;1→r14→r15
94: (N/r10)(J-1)→r9
95: if r9>r4;-1→r14;r1-r9→r9
96: if r9>r5;-1→r15;r4-r9→r9
97: r9+1→r12;r5-r9+1→r13
98: for I=J to N by r10
99: r15C[r13]→r16;r14C[r12]→r17
100: I+r11→r18
101: X[r18]r16+Y[r18]r17→r7;-X[r18]r17+Y[r18]r16→r8
102: X[I]-r7→X[r18];Y[I]-r8→Y[r18]
103: X[I]+r7→X[I];Y[I]+r8→Y[I];next I;next J;next L
104: for I=1 to N;X[I]/4N→X[I];Y[I]/4N→Y[I]
```

hanning window used to reduce energy leakage resulting from truncation (due to a finite time record) of data

actual FFT algorithm where block size is 2*N*; real data is stored in X array; complex transform is stored as X + i Y except that A[1] is the real d.c. component and B[1] is the real maximum frequency component

```
105: next I
106:
107: "com":N/2+1→r3;N/4+2→r4
108: C[r4]→r5;C[r4+1]→r6
109: for I=1 to r3;I-2int(I/2)→r18
110: if r18=1;gto +3
111: I/2→r7;C[r4-r7]→r8;C[r7]→r9
112: r9r6+r8r5→r11;r8r6-r9r5→r10;gto +2
113: C[(I+1)/2]→r11;C[(r3-I)/2+1]→r10
114: N-I+2→r12
115: if r12#N+1;gto +3
116: 4/2→r13;X[1]→r14
117: (r14+Y[1])r13→X[I];(r14-Y[1])r13→Y[1];gto +5
118: X[I]→r14;X[r12]→r15;Y[I]→r16;Y[r12]→r17
119: r14+r15+r11(r15-r14)+r10(r16+r17)→X[I]
120: r16-r17-r11(r16+r17)+r10(r15-r14)→Y[I]
121: Y[I]-2(r16-r17)→Y[r12];2(r14+r15)-X[I]→X[r12]
122: next I
```

actual FFT algorithm where block size is 2N; real data is stored in X array; complex transform is stored as X + i Y except that A[1] is the real d.c. component and B[1] is the real maximum frequency component

```
123:
124: for I=2 to N;X[I]↑2+Y[I]↑2→X[I];if X[I]=0;1e-9→X[I]
125: next I
```

N points of real frequency data calculated in X array

```
126:
127: "find the carrier":F2N/R→X
128: X[X]→M;X+10→H;X-10→L
129: if N<H;N→H
130: for I=L to H
131: max(X[I],M)→M
132: next I
133: for I=L to H
134: if X[I]=M;gto "find all carrier"
135: next I
```

carrier line calculated

```
136: "find all carrier":
137: I→X;X+10→H;X-10→L
```

width of carrier determined

```
138:
139: "find max point outside of carrier":
140: 0→G;for I=3 to N
141: if I<L or I>H;max(G,X[I])→G
142: next I
```

maximum signal level not including d.c. component or carrier signal is determined as maximum noise

```
143: fxd 1;prt "Peak noise=",10log(G/M),"dBc";spc 2
```

peak noise printed

```
144:
145: ent "plot FFT?(yes=1)",J
146: if J#1;gto "end"
```

continue if plot desired

```
147:
148: "Plot FFT":
149: dsp "plot FFT"
150: psc 705
```

plotter select code

```
151: scl -2,R/2+1,-110,50;line
152: pen# 1
153: for I=2 to N
154: plt R(I-1)/2N,max(10log(X[I]/M),-90);next I
155:
```

FFT frequency data plotted

```
156: pen# 2
157: line 3
158: if F<R/2-1;yax R(H-1)/2N,0,-90,0
159: yax R(L-1)/2N,0,-90,0
160: line
161:
162: pen# 3
163: csiz
164: fxd 1
165: xax -90,1,0,R/2,1
166: fxd 0;yax 0,10,-90,10,1;yax R/2,10,-90,10
167: csiz 2;plt R/6,-107,1;lbl "Frequency(MHz)"
168: deg;csiz 2,2,1,90;plt -1,-60,1;lbl "Spurious Level(dBc)"
169: plt R(L-10)/2N,1,1;csiz 1.5
170: if F>.4R;plt R(L-20)/2N,1,1
171: lbl "fundamental"
172: plt .5,37,1
173: csiz 2.5;lbl "5180 FFT PLOT"
174: cplt ;fxd 2;csiz 2
175: lbl "Frequency=",F,"MHz Channel",C
176: cplt ;fxd 1
177: lbl "Peak noise=",10log(G/M),"dBc"
178: pen# 0
179:
180: end
*30096
```

carrier width plotted

axes plotted

labels plotted

lift plotter pen

APPENDIX G

TYPICAL THEORETICAL PARAMETERS OF A TRANSIMPEDANCE AMPLIFIER

The most striking aspect of a transimpedance amplifier is the manner in which the bandwidth and high speed performance have been separated from the actual circuit gains and configurations. The result is a realiable device that comes much closer to the "ideal" amplifier without performance trade-offs.

Gain insensitive bandwidth is largely a result of the current feedback versus the traditional voltage feedback technique. An additional benefit of the transimpedance structure is slew rates up to 7500 V/usec which allows the output to swing a full ± 10 volts up to 60 MHz. Superior settling times (10 nsec to 0.1%).

Understanding the Transimpedance Amplifier

The transimpedance amplifier operates like a standard voltage input differential amplifier in terms of settling gain and calculating noise. The primary difference between the two amplifier types is the low impedance inverting input, which causes current feedback instead of voltage feedback. The result is a deviation from the inverse relationship between gain and bandwidth of traditional amplifier designs. Figure G.1 portrays the model used in the analysis that follows. R_{in} and R_f are the usual gain setting resistors, R_s is the internal input resistance (impedance) of the amplifier. Two equations are required to describe the operation of this amplifier. Equation G1 is a generic amplifier transfer function. Equation G2 sums the currents at the inverting input.

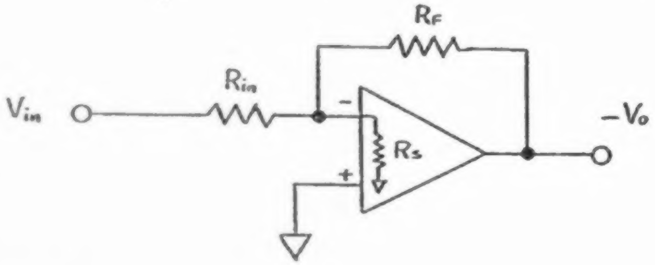


FIGURE G.1 AMPLIFIER MODEL

$$-V_o = A(w)\,V_{in} \qquad \text{eq.(G1)}$$

$$\frac{V_s - V_{in}}{R_{in}} + \frac{V_s}{R_s} + \frac{V_s - V_o}{R_F} = 0 \qquad \text{eq.(G2)}$$

rearranging equation G2 provides:

$$V_s\left[\frac{1}{R_{in}} + \frac{1}{R_s} + \frac{1}{R_F}\right] = \frac{V_o}{R_F} + \frac{V_{in}}{R_{in}}$$

Reducing further:

$$V_s = \left[\frac{R_{in}R_s}{R_sR_F + R_{in}R_F + R_{in}R_s}\right]V_o + \left[\frac{R_sR_F}{R_sR_F + R_{in}R_F + R_{in}R_s}\right]V_{in}$$

letting $K = R_sR_F + R_{in}R_F + R_{in}R_s$ and substituting results

$$V_s = \left[\frac{R_{in}R_s}{K}\right]V_o + \left[\frac{A(w)\;R_FR_s}{K}\right]V_{in}$$

substituting from eq. G1 above, we obtain

$$-V_o = \left[\frac{A(w)R_{in}R_s}{K}\right]V_o + \left[\frac{A(w)R_FR_s}{K}\right]V_{in}$$

which leads to equation G3 below:

$$-\frac{V_o}{V_{in}} = \left[\frac{A(w)\;R_sR_F\;/\;K}{1 + A(w)\;R_{in}R_s\;/\;K}\right] \qquad \text{eq.(G3)}$$

and since $(\,1 + A(w)\;R_{in}R_s\;/\;K\,) \approx A_oR_{in}R_s\;/\;K$ then:

$$-\frac{V_o}{V_{in}} = \left[\frac{G}{1 + jwtK\;/A_o\;R_{in}R_s}\right]$$

Now replacing K and noting that R_f/R_{in} = G (close loop gain) we obtain:

$$-\frac{V_0}{V_{in}} = \left[\frac{G}{1 + jwtR_f/A_0 \quad 1/R_{in}+1/R_s+1/R_f}\right]$$

At this point the difference between the transimpedance and traditional amplifiers becomes evident. For traditional voltage input amplifiers the input resistance, R_s approaches infinity; accordingly $1/R_s$ approaches 0. The term R_f $(1/R_{in} + 1/R_s + 1/R_f)$ simplifies to $[R_f\ (1/R_{in} + 1/R_f)]$ which further reduces to (G + 1). Substituting we obtain the final relationship for the traditional amplifier design. The transimpedance amplifier provides a dramatically different result. The value of R_s is not large; (approximately 20 Ohm). Noting that $R_{in}//R_s//R_f$ and since $R_s <<< R_{in}$ and/or $R_f\ (1/R_{in} + 1/R_s + 1/R_f) = 1/R_s$. Substituting we obtain the relationship comparable with that developed for the traditional amplifier above.

$$-\frac{V_0}{V_{in}} = \left[\frac{G}{1 + jwt/A_0\left[R_f/R_s\right]}\right] \qquad \text{TRANSIMPEDANCE AMP.}$$

$$-\frac{V_0}{V_{in}} = \left[\frac{G}{1 + jwt/A_0\left[G + 1\right]}\right] \qquad \text{TRADITIONAL OP-AMP.}$$

The two amplifier types yield similar algebraic results with one dramatic difference. The traditional relationship shows that the closed-loop gain (G) is multiplied directly by the frequency dependent term in the denominator, thus accellerating the gain roll-off as frequency increases. In the transimpedance, the frequency dependent term is multiplied by the constant R_f/R_s, causing the bandwidth to remain steady for a given feedback resistor. The characteristic closed-loop frequency response plots for the two amplifier types differ markedly.

Note that for a traditional one pole amplifier Figure G.2, as the closed-loop gain increases, the bandwidth diminishes dramatically.

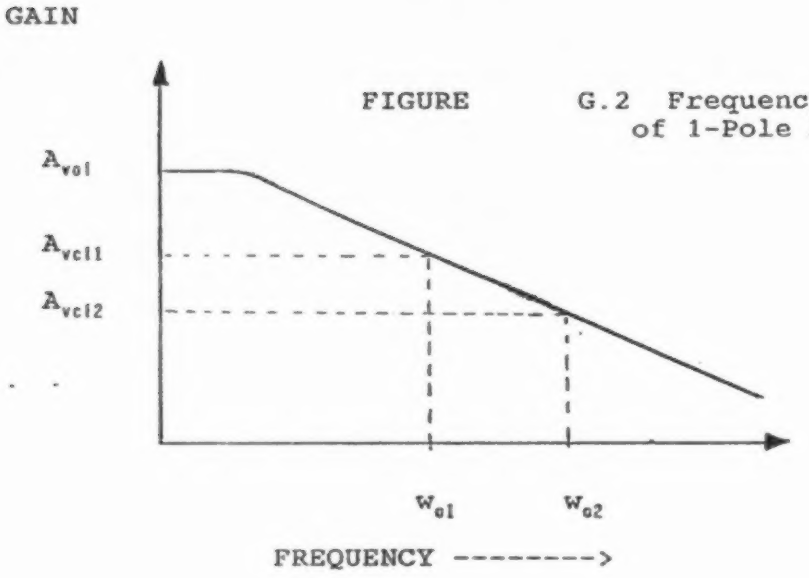


FIGURE G.2 Frequency response of 1-Pole Amplifier

The frequency response of the transimpedance amplifier Figure A-3, change very little when the gain is changed. The closed-loop gain changes when a new gain setting is chosen, but the -3 dB bandwidth changes very little for the various gain settings.

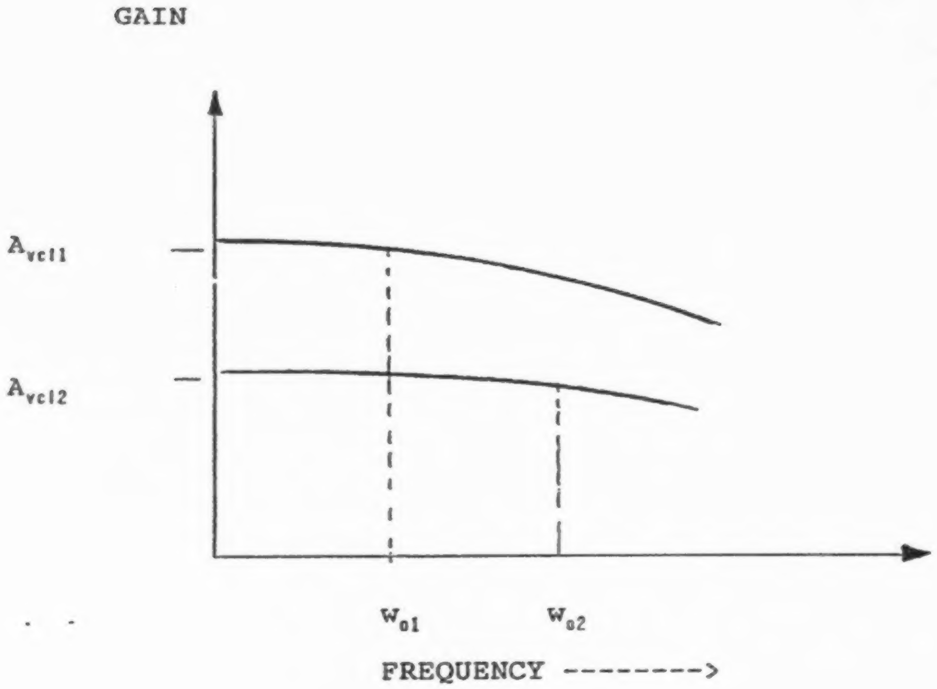


FIGURE G.3 FREQUENCY RESPONSE OF A TRANSIMPEDANCE AMPLIFIER

APPENDIX H

DESCRIPTION OF NOISE FIGURE AND THIRD ORDER INTERCEPT POINT RELATIONSHIP FOR SELECTION OF DESIGN PARAMETERS

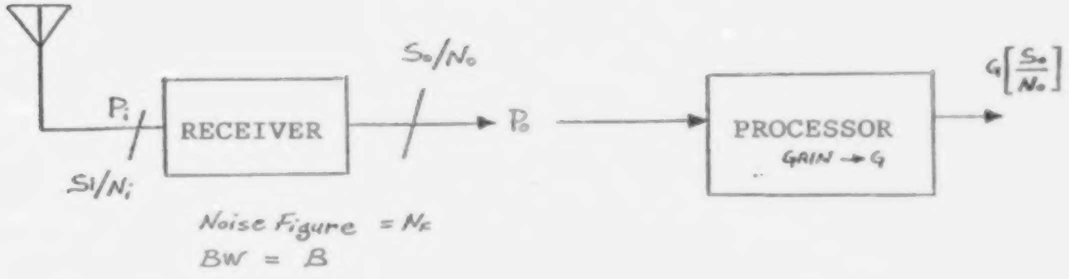


FIGURE H.1 RECEIVER SYSTEM

For a bandwidth B_1 and receiver noise figure N_1 we have a sensitivity of S_1 based on a (S+N)/N ratio of 3 dB where:

$$S_1 = 174 \text{ dBm} + 10 \log (B_1) + N1 \qquad \text{eq. (H1)}$$

basically this is the noise floor as shown in H.2

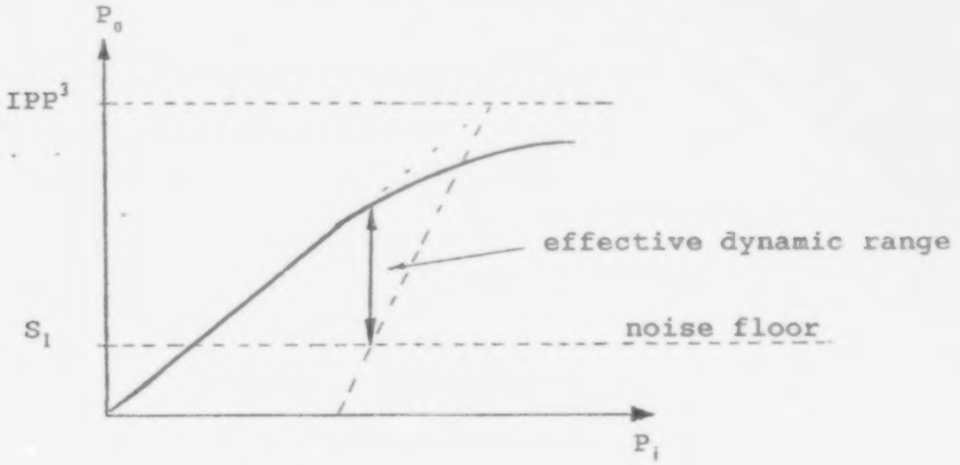


FIGURE H.2 RECEIVER INPUT-OUTPUT TRANSFER FUNCTION

for a spuriour free dynamic range we have:

$$SFDR < 2/3 \; (IIP^3 - S_1) \qquad \text{eq.(H2)}$$

we have:

$$IIP^3 \geq N_f + (3/2(SFDR) + [-174 \text{ dBm} + 10 \log (BW)]) \quad \text{eq. (H3)}$$

- we can see that inequality H3 has the form $Y \geq x + a$. Therefore, if we plot this inequality for constant B_1 and SFDR we have a graph that looks like Figure H3.

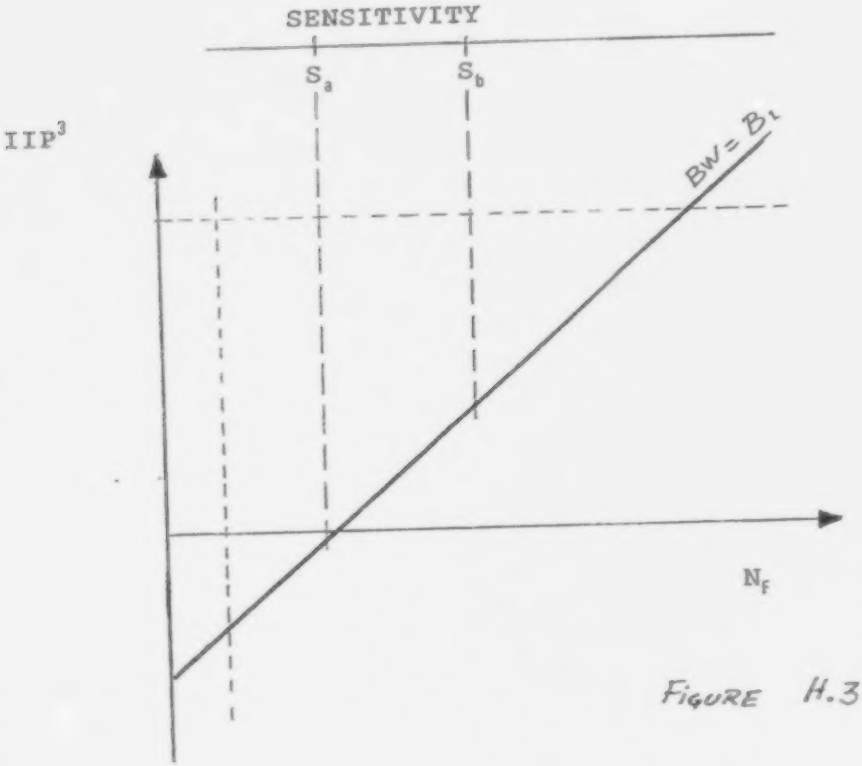


FIGURE H.3

What this tells us is that any value of IPP^3 above the $Y \geq x+a$ line will give us an SFDR $\geq$ D dB where D is a value which we would like to achieve.

This inequality is used only to illustrate some of the design constraints that we are facing on a front end implementation. Note also the constraints added by the technology of components (state of the art lines). The area bounded by all these inequalities gives us a design freedom in choosing the available components for a front-end design. As a result, if the area is small, we would expect to have difficulties in implementation. We are going to illustrate this with an example. The example is already shown in Figure 2.3.2.

Here we have a bandwidth of 58 MHz (88 MH - 30 MHz) and we would like an SFDR of 48 dB which gives a signal to noise ratio of 48 dB at the input of an 8 bit A/D.

Therefore, equation H3 becomes:

$$IPP^3 \geq N_F - 24.3 \quad \text{dBm}$$

The sensitivities axis illustrates the range of input signals expected for different noise figures, i.e.

$$S = -96.4 + N_F \quad \text{dBm}$$

Note that in Figure 2.3.2 the sensitivity axis helps in determining other constraints in the design. For example one of the constraints could be that sensitivity should be within S_a and S_b with no processing gain.

Note in Figure H.1 that if we have a processing gain G, then the signal to noise ratio S_0/N_0 could be improved by G dbs (i.e. during digital processing, there is no noise added by a processor).

This is equivalent to say that for the same signal to noise ratio S_0/N_0 with a processing gain, we could detect smaller signals or in other words, the receiver is G dB more sensitive.

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